Chapter 5

Digital Electronics

5.1 Superconductivity and Digital Electronics

Potential Advantages and Disadvantages

Fast (< 100 GHz)

Low-power (aJ / gate)

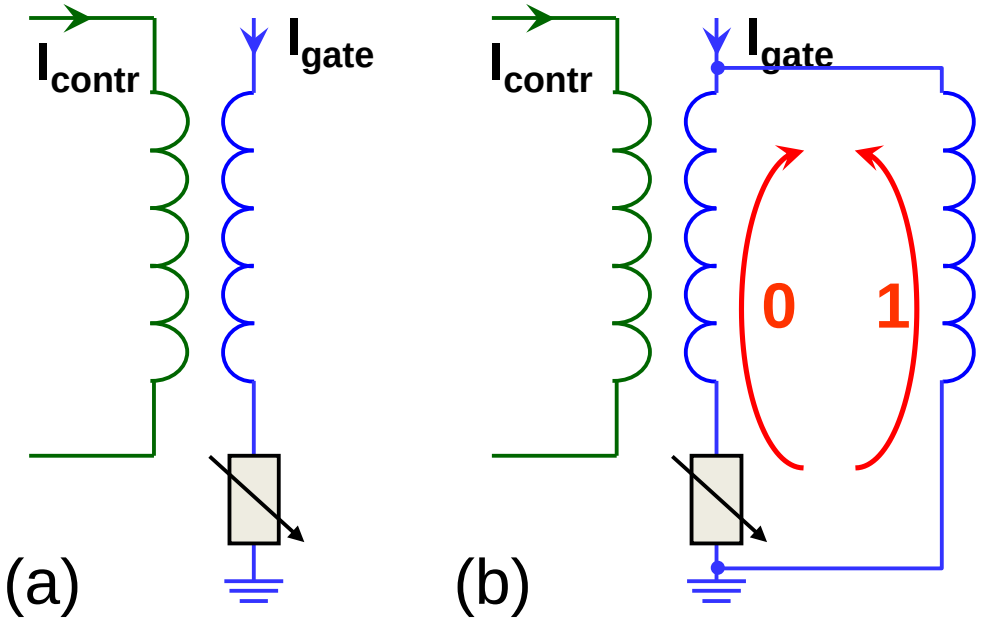
Requires cooling

Not yet established technology

Requires new periphery (power supply, packaging, ...)

5.1.1 Historical Development

The Cryotron (1956)



Operating principle: superconducting-normal transition in wire

Control line has higher critical magnetic field

Control line switches enough current to control another gate → Logic

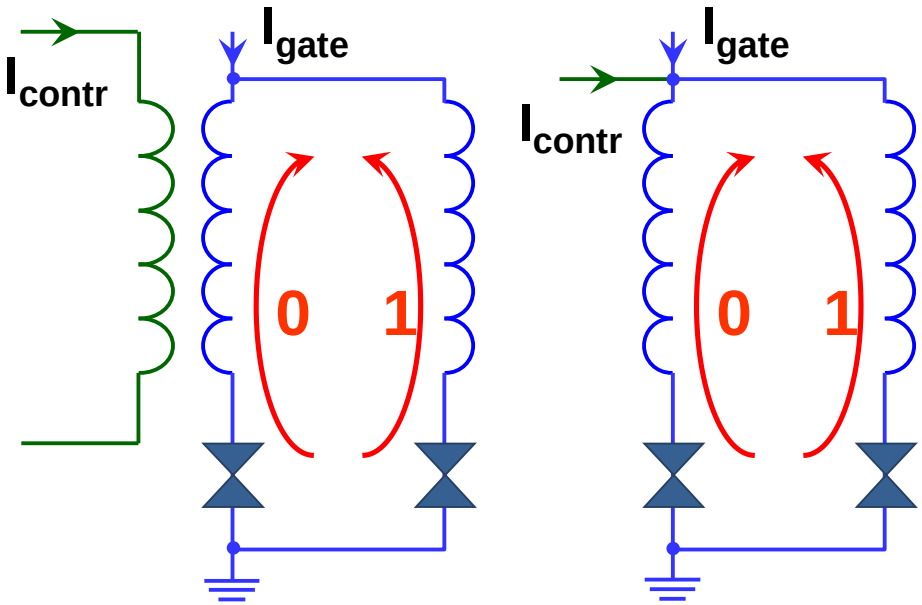
Memory: trap flux $\pm\Phi$ in loop, read/write via sc-normal transition

Inferior to semiconductor devices (low switching speed $\tau_{LR} \simeq 10$ ns)

5.1.1 Historical Development

The Josephson Switch (1966, Matisoo, IBM)

Increase τ_{LR} by switching JJ or SQUID instead of sc wire → Josephson cryotron



Sub-ns switching times → Clock speeds up to 1GHz

Control → Flux quantum as natural bit

Strong shielding and controlled trapping of residual flux required

Underdamped Pb junctions → Large I_c-spread, vulnerable to thermal cycling

→ IBM stops efforts in 1983

5.1.1 Historical Development

Rapid Single Flux Quantum (RSFQ) Logic (1985, Likharev, Nakajima)

Operating principle:

Non-latching logic with overdamped Nb-JJ
Slightly above I_c → ps current pulses
Phase difference evolves by 2π during pulse
Use resulting voltage pulses for logic circuits

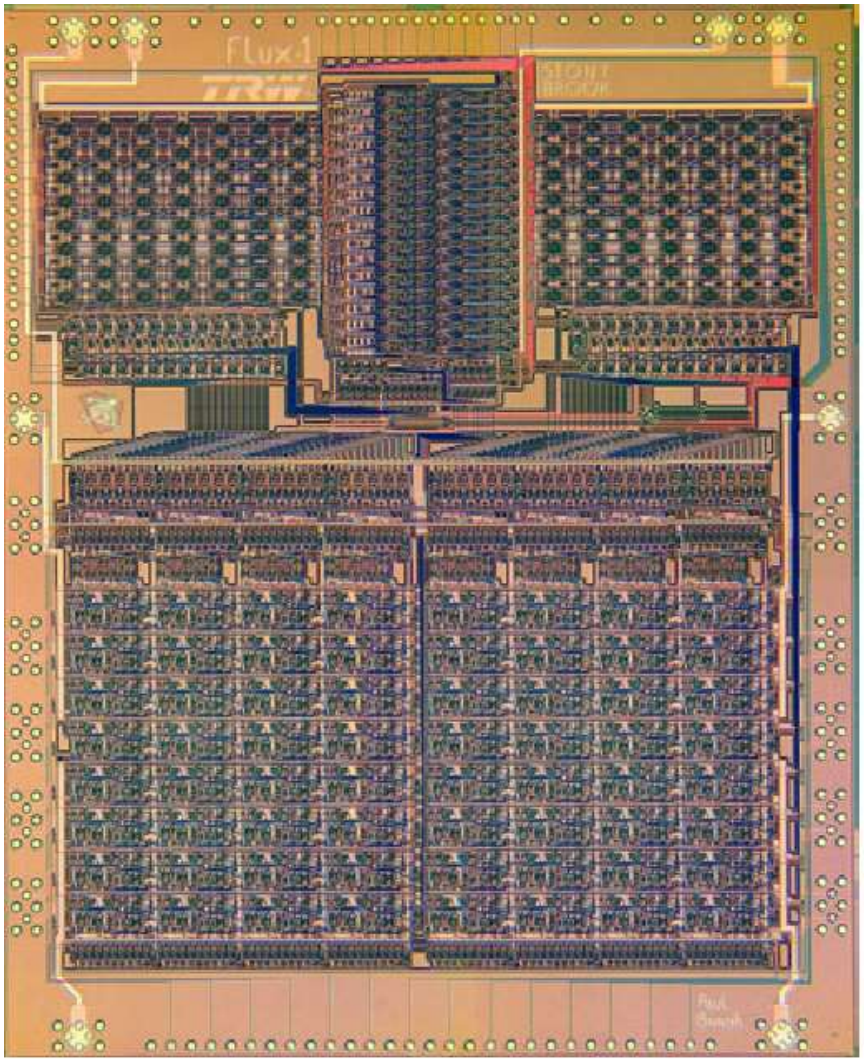
1978 → First RSFQ gate (T-flip-flop) proposed

Fast (record so far: 770 GHz clock speed)
Intrinsic memory
Low power consumtion
Reproducible fabrication possible

Fabrication still demanding
No transistor-like superconducting devices with high gain
→ High fan-out difficult
→ Small parameter spread required

5.1.1 Historical Development

Rapid Single Flux Quantum (RSFQ) Logic (1985, Likharev, Nakajima)



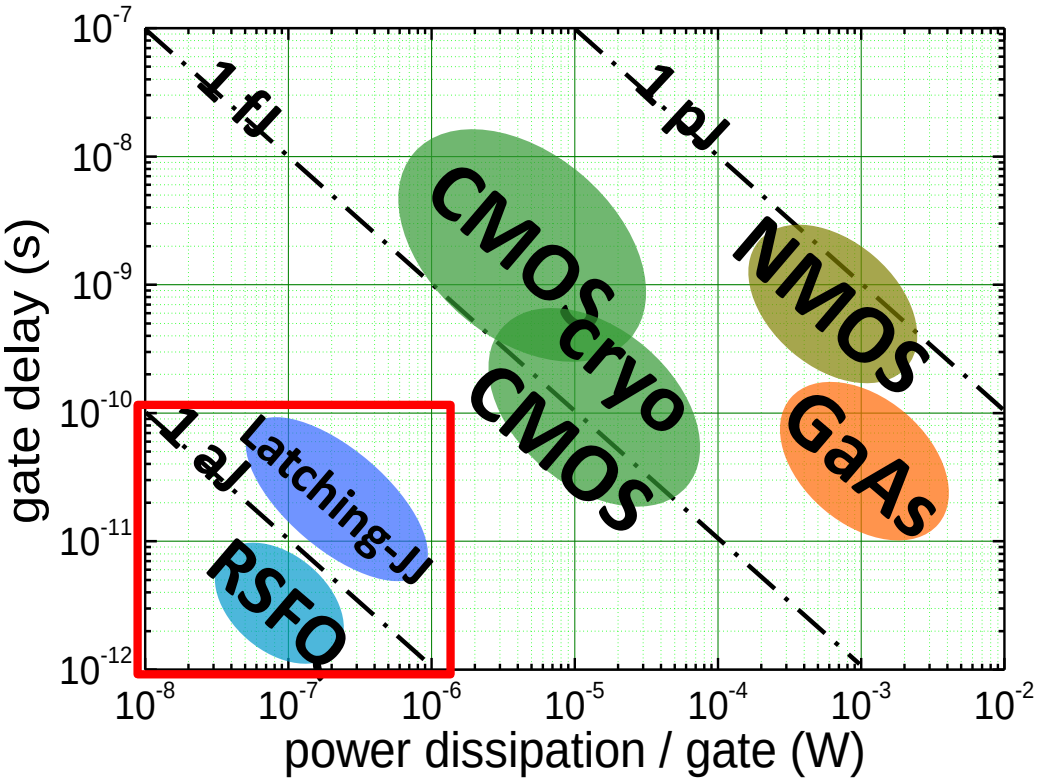
FLUX-1

- the first RSFQ MPU
- 8 bit ALU array
- 16 word instruction memory
- 70,000 JJs
- 14 mW
- 20-22 GHz @ F = 2.0 um

  ($\Rightarrow$ 120-140 GHz @ 0.3 um)
- TRW's 4-metal process

5.1.2 Advantages of Josephson Switching Devices

Fast



Low power

		1 user		10^7 users	
		dissipated power at clock speed		dissipated power at clock speed	
	$P_{diss} \cdot \tau$	1 GHz	1 THz	1 GHz	1 THz
Si	1 nJ	1 Watt	1000 Watt	10^7 Watt	10^{10} Watt
Josephson	1 pJ	1 mWatt	1 Watt	10^4 Watt	10^7 Watt

(For 10^6 switching elements)

5.1.2 Advantages of Josephson Switching Devices

Matched superconducting striplines for on-chip wiring (fast, low dissipation)

$$Z\,[\Omega] \;=\; 60\,\frac{\sqrt{t_I t_M}}{W\sqrt{\epsilon}}\;, \qquad t_M \;=\; t_I + 2\mathrm{Re}\delta$$

$Z \simeq 10\ \Omega$ close to JJ resistance for width $W \simeq 1\ \mu\mathrm{m}$
Little dispersion up to 1 THz → Transfer of ps pulses OK
Dense layout with little crosstalk possible

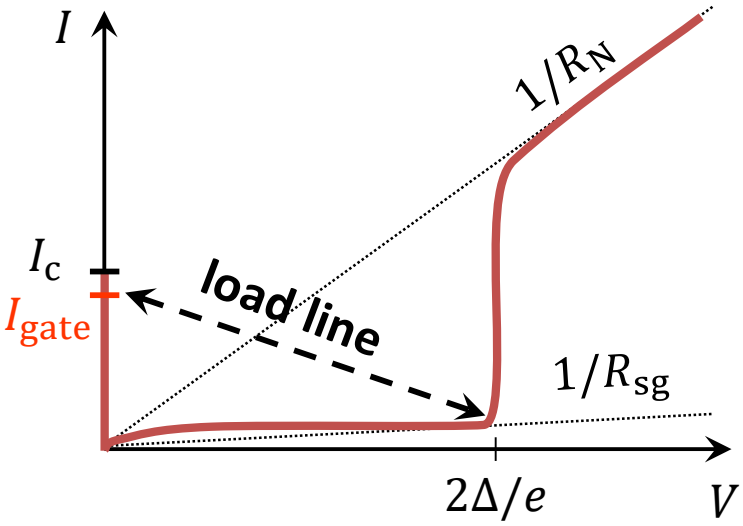
Junction technology available (Nb based)

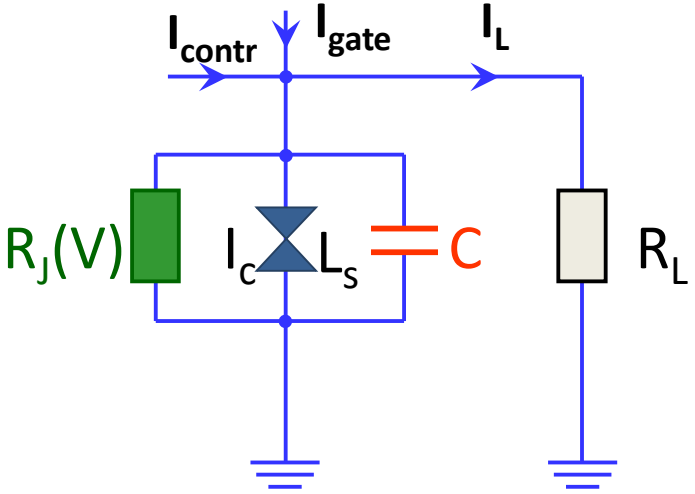
5.2 The voltage state Josephson logic

Underdamped JJ as switching gates

→ Zero and finite voltage state as 0 an 1

→ Natural emulation of semiconductior logic





Initially: $I_{\mathrm{gate}} < I_{\mathrm{c}}$

$I_{\mathrm{contr}} + I_{\mathrm{gate}} > I_{\mathrm{c}}$ → Switching

Load $R_{\mathrm{L}} \ll R_{\mathrm{sg}}$ → All current transferred to load after switching

5.2.1 Operation Principle and Switching Times

Characteristic Times (linearized LCR circuit)

$$L_s = \frac{\Phi_0}{2\pi I_c \cos\varphi(t)} = \frac{L_c}{\cos\varphi(t)} \qquad \text{with} \qquad L_c = \frac{\Phi_0}{2\pi I_c} = \frac{\hbar}{2eI_c}$$

$$\tau_{RC} = RC$$
$$\tau_{LR} = L_c/R = \Phi_0/2\pi I_c R$$

$$1/R(V) = 1/R_L + 1/R_J(V)$$

Geometric mean

$$\tau_{LC} = \sqrt{L_c C} = \sqrt{\Phi_0 C/2\pi I_c} = \sqrt{\tau_{RC}\tau_{RL}}$$

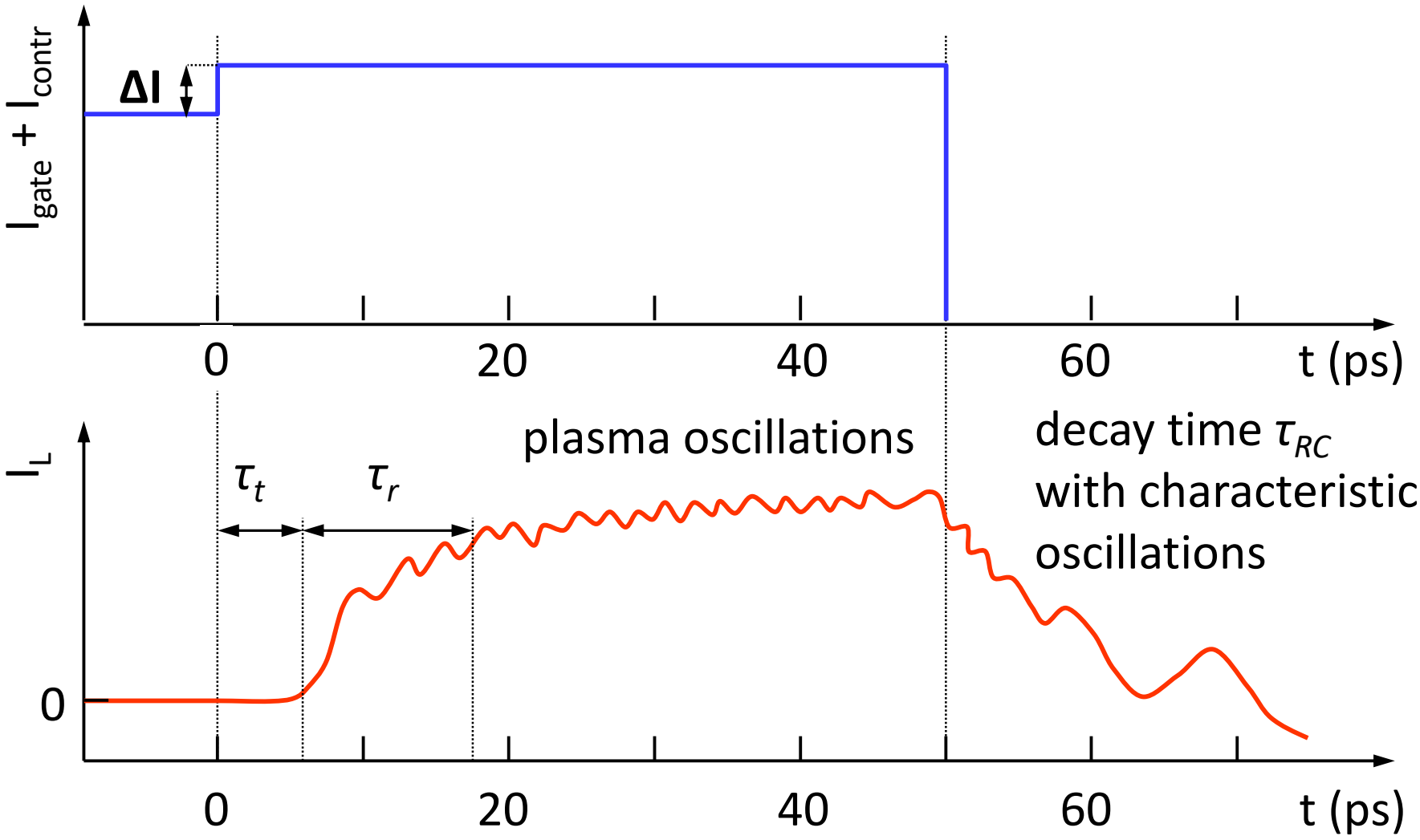
Underdamped junction for switching logic

$$\beta_C = \tau_{RC}/\tau_{RL} > 1 \quad \rightarrow \quad \boxed{\tau_{RC} > \tau_{LC} > \tau_{RL}}$$

→ Switching time limited by τ_{RC}

5.2.1 Operation Principle and Switching Times

Computer simulation for underdamped switching junction
(parameters see lecture notes)



5.2.2 Power Dissipation

for Nb junction:

$$P_{\text{diss}} = \frac{V_g^2}{R_{sg}}$$

$$R_{sg}^{th} \lesssim \frac{V_g}{I_c^{th}} \times 10 \simeq 30\,\Omega$$

$$P_{\text{diss}} \simeq 3 \times 10^{-7}\,\text{Watt}$$

$$E = P_{\text{diss}} \cdot \tau \simeq 3 \times 10^{-18}\,\text{J}$$

Compare to semiconducting devices & HTSL →

material	$P_{\text{diss}} \cdot \tau$ (Joule)
Si	$10^{-8} - 10^{-10}$
GaAs	$10^{-8} - 10^{-10}$
HEMT	$10^{-10} - 10^{-11}$
HTSL	3×10^{-15}

5.2.3 Global Clock, Punchthrough

Voltage state logic → Underdamped JJ

1. Latching nature requires to switch off bias current
   → Global clock system at GHz frequecies required

2. Ac power source required
   → JJ biased with ac current source
      → Shapiro steps
      → JJ may switch back to step voltage instead of zero
   → Bipolar operation
      → JJ may switch through to negative voltage branch
      → „Punchthrough“
      → Intrinsic feature of Josephson physics
      → Limits clock speed to a few GHz
         → No speed gain over semiconductor technology!

5.2.4 Josephson Logic Gates

General requirements

High fan-out

→ Single gate should trigger multiple consequtive gates

Large parameter margins

→ Stable operation

Small size

→ Very large scale integration

Short gate times

→ High clock frequency

→ Requires fast switching

Low power dissipation

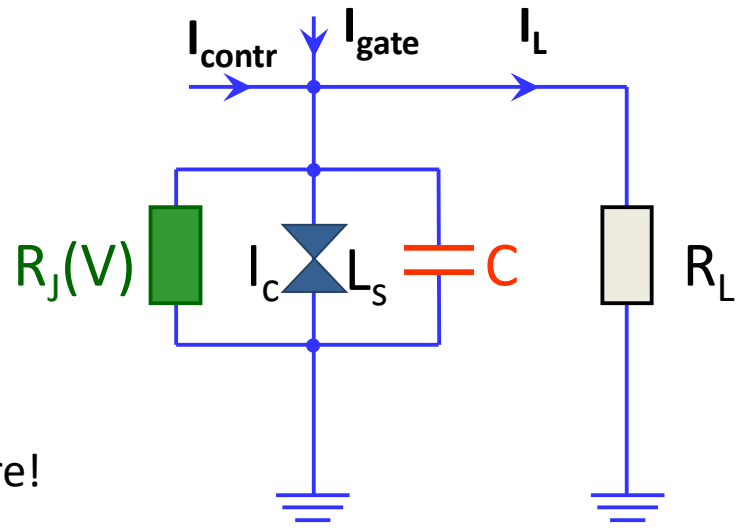
→ High integration density

Input-output isolation

→ Directional logic

→ Difficult in switching gates

→ Not satisfied by simple circuit shown before!



5.2.4 Josephson Logic Gates

Performance (see lecture notes for details)

Table 5.1: Switching delay and power dissipation for various types of logic gates.

gate	linewidth (μm)	switching time (ps)	power dissipation (μW)	junction technology	Ref.
CIL	2.5	13	2	Pb-alloy	*a*
JAWS	5	13		Pb-alloy	*b*
RCJL	5	10.3	11.7	Pb-alloy	*c*
RCL	2	4.2		Pb-alloy	*d*
4JL	2.5	7	4	Pb-alloy	*e*
DCL	1.5	5.6	4	NbN/Pb-In	*f*
MVTL	1.5	2.5	4	Nb/AlO_x/Nb	*g*

[a] T.R. Gheewala, A. Mukherjee, in *Tech. Digest International Electron Device Meeting (IEDM)*, p. 482 (1979).
[b] S.S. Pei, Appl. Phys. Lett. **40**, 739 (1982).
[c] J. Sone, T. Yoshida, S. Tahara, H. Abe, Appl. Phys. Lett. **41**, 886 (1982).
[d] J. Nakano, Y. Mimura, K. Nagata, Y. Hasumi, T. Waho, in *Ext. Abstr. of 16th Conf. Solid State Dev. and Mat.*, Kobe (1984), p. 636.
[e] H. Nakagawa, T. Odake, E. Sogawa, S. Takada, H. Hayakawa, Jap. J. Appl. Phys. **22**, L297 (1983).
[f] Y. Hatano, T. Nishino, Y. Tarutani, U. Kawabe, Appl. Phys. Lett. **44**, 1095 (1984).
[g] S. Kotani, T. Imamura, H. Hasuo, in *IEEE IEDM Tech. Digest*, p. 865 (1987).

Speed not due to gate type, but due to junction technology
(typical gate speed for Nb technology)

5.2.5 Memory Cells

General definitions and requirements

General types

NDRO: Non-Destructive Read-Out

DRO: Destructive Read-Out

Speed requirements

Order of CPU speed

Natural physical quantity

persistent currents / magnetic flux in sc.loops

„0“: no flux in the loop

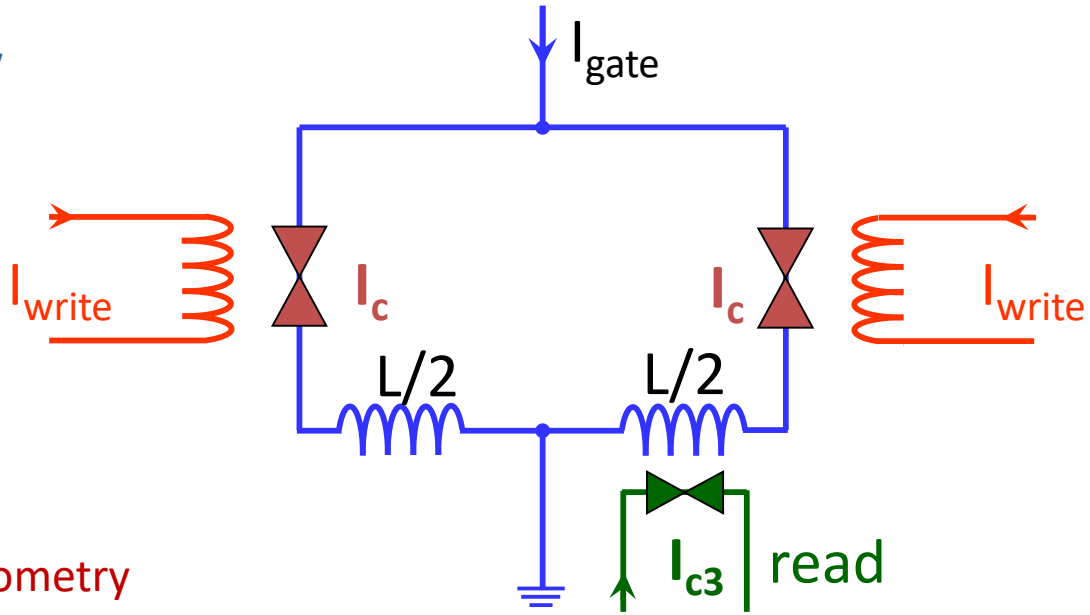
„1“: finite flux in the loop (usually Φ_0)

Access

Read/write JJ-based gates

5.2.5 Memory Cells

NDRO memory



Dc-SQUID geometry

WRITE operation

Finite bias I_{gate}

→ No flux coupled into loop at $I_{\text{write}} = 0$

→ Increase I_{write} such that induced shielding current $I_{\text{sh}} > I_{\text{c}}$

Turn off I_{write} → Flux remaines trapped for $\beta_L > 1$

READ operation

JJ_3 biased slightly below I_{c3}

„0“ state → No circulating current → No switching of JJ_3

„1“ state → Circulating current suppresses I_{c3} → Switching of JJ_3

Does not alter cell state

5.2.5 Memory Cells

Performance

access time	380 ps
power dissipation	9.5 mW
bit yield	99.8 %
Josephson junctions	$Nb/AlO_x/Nb$
number of junctions	21.000
cirtical current density	$3.3\,kA/cm^2$
minimum junction size	$2\,\mu m \times 2\,\mu m$
minimum line width	$1.5\,\mu m$
cell size	$55\,\mu m \times 55\,\mu m$
RAM size	$4.5\,mm \times 4.5\,mm$

Table 1.3: Josephson 4 kbit RAM characteristics (Organization: 4096 word x 1 bit, NEC)

Still inadequate for most applications (too big)
1996 an $8.5 \times 11.5\ \mu m^2$ chip ($1\ Mb/cm^2$) demonstrated
(Compare: 2016 Samsung 3D NAND flash →$185\ Gb/cm^2$)

5.2.6 Problems of Underdamped Junction Logic

Underdamped junction logic gates and memory → Josephson microprocessors were built

Problems preventing their practical use

Pb technology too unreliable → Solved with Nb technology

Latching logic

- Ac power supply and global timing required
- Speed < 1GHz due to punchthrough
- Switching back to zero voltage state slow (~1 ns)

No transistor-like amplifying 3-terminal device

5.3 RSFQ Logic

Specific properties of RSFQ logic

Acronym for rapid single flux quantum logic

Clock frequencies above $100\ \mathrm{GHz}$ → Fast!

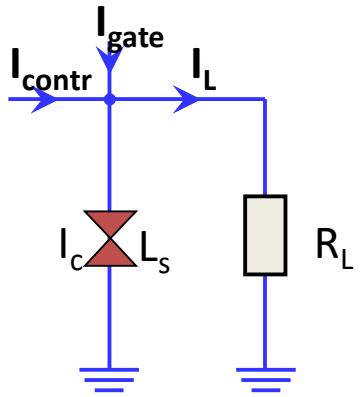
Nonlatching logic

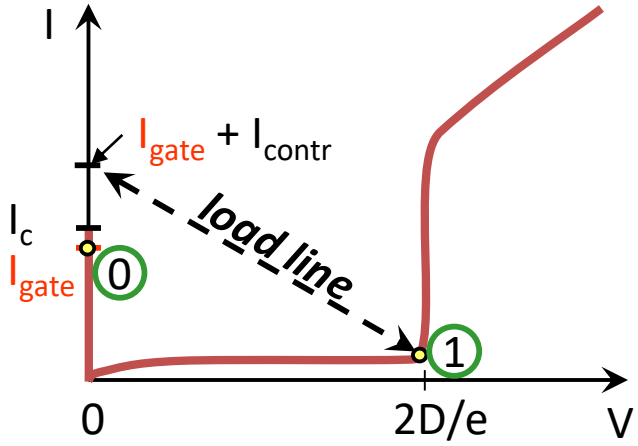
Overdamped Josephson junctions

Low power consumption $P_{\mathrm{diss}}\tau \simeq 10^{-18}\,\frac{\mathrm{J}}{\mathrm{bit}}$

5.3 RSFQ Logic

Switching vs. RSFQ logic





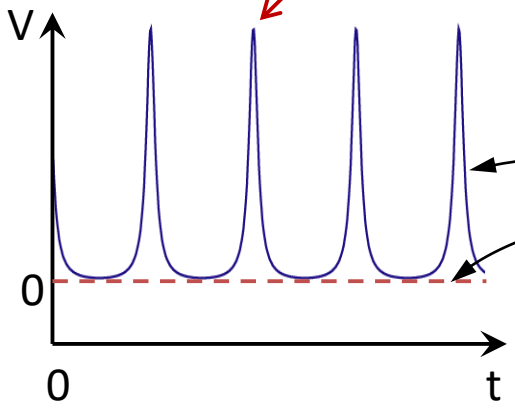
Latching

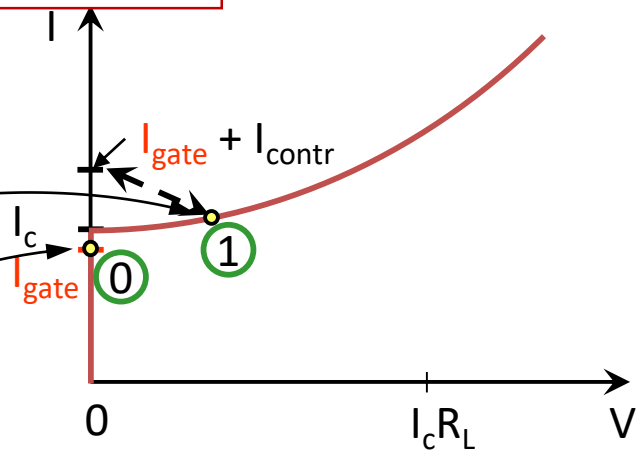
„0“ → „1“ fast

„1“ → „0“ slow

→ Not competitive with semiconductor-based logic

$$\int V\,dt = \int \frac{\hbar}{2e}\,d\varphi = \frac{h}{2e} = \Phi_0 = 2.07 \times 10^{-15}\ \mathrm{Vs}$$





Nonlatching

„0“ → no SFQ emitted

„1“ → SFQ emitted

→ Significantly faster than semiconductor-based logic

SFQ pulses can be naturally generated, reproduced, amplified, memorized and processed with overdamped Josephson junctions!

5.3 RSFQ Logic

Static SFQ circuits

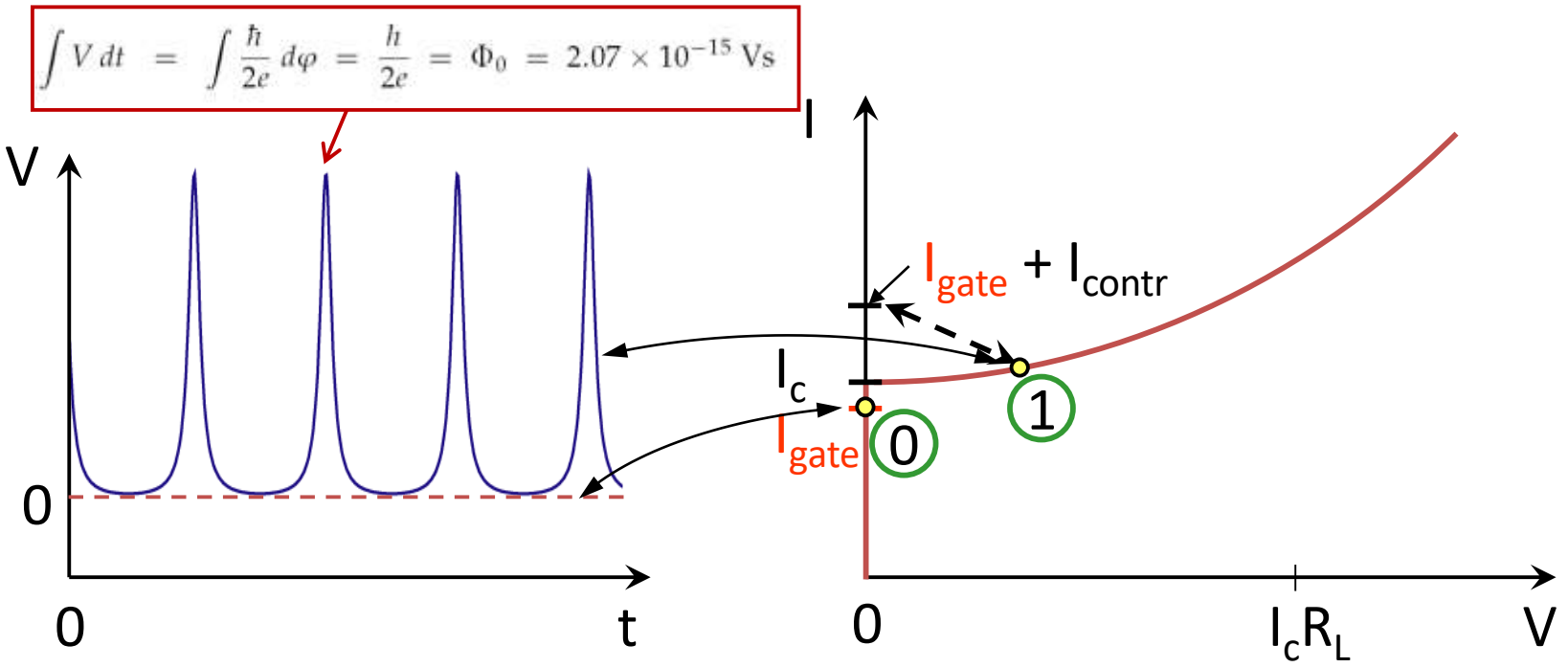
Information passed as dc flux/supercurrent

→ Limited integration, requires rf power supply/clock → Practical limitations!

Dynamic SFQ circuits

Information passed ballistically between devices

Interconnects → Micostrip (passive) or Josephson transmission lines (active)



5.3 RSFQ Logic

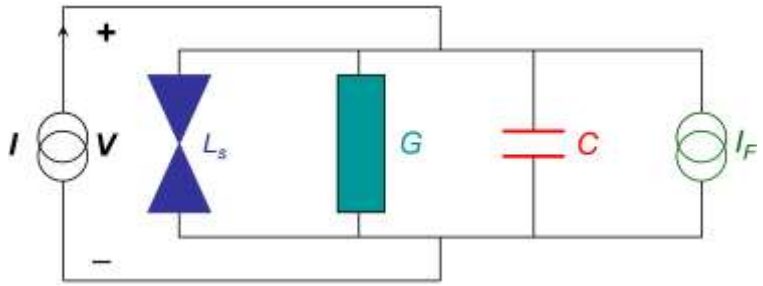
Repetiton: Voltage state of overdamped JJ

T: oscillation period

Time averaged voltage

$$\langle V\rangle = \frac{1}{T}\int_0^T V(t)\,dt = \frac{1}{T}\int_0^T \frac{\hbar}{2e}\frac{d\varphi}{dt}dt = \frac{1}{T}\frac{\hbar}{2e}\overbrace{[\varphi(T)-\varphi(0)]}^{2\pi} = \frac{\Phi_0}{T}$$

Total current must be constant (neglecting the fluctuation source)



$$I = I_s(t) + I_N(t) + I_D(t)$$

and $$\varphi(t) = \int_0^t \frac{2e}{\hbar}\,V(t)\,dt$$

$I > I_c$

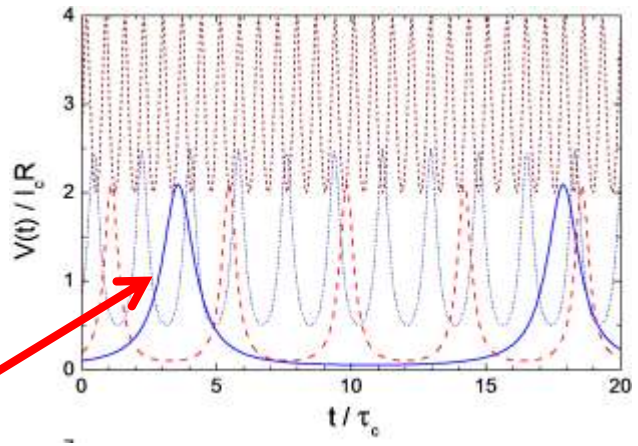
→ Part of the current as I_N or I_D

→ Finite junction voltage $|V| > 0$ → Time varying I_s

→ $I_N + I_D$ varies in time → Time varying voltage

→ Sinusoidal or non-sinusoidal oscillations of I_s

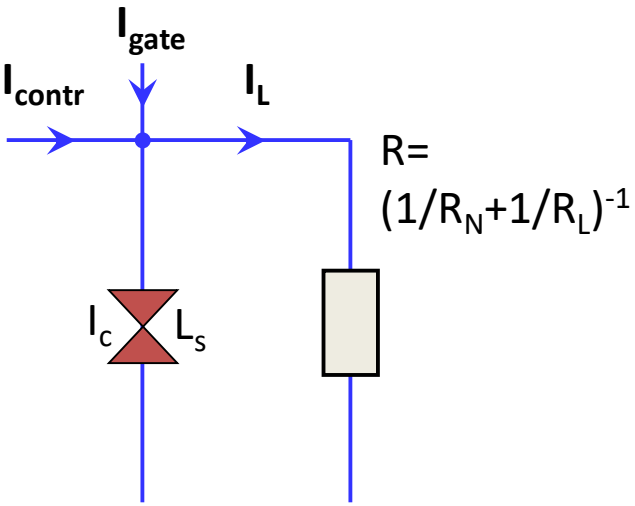
→ Oscillation frequency $f = \frac{h\langle V\rangle}{\Phi_0}$

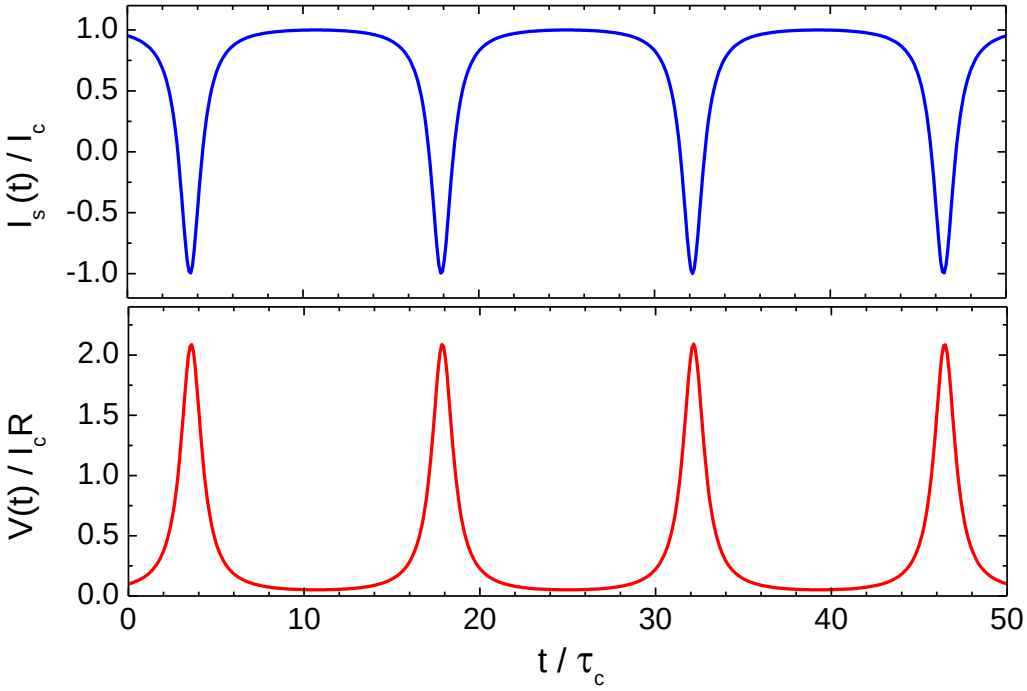


RSFQ pulse

5.3.1 Basic Components of RSFQ Circuits

Generation of RSFQ pulses – single JJ





Bias overdamped JJ sightly above I_c

→ Pulse duration $\Phi_0/2I_cR \approx 1$ ps for $I_cR \approx I_cR_N \approx 1$mV

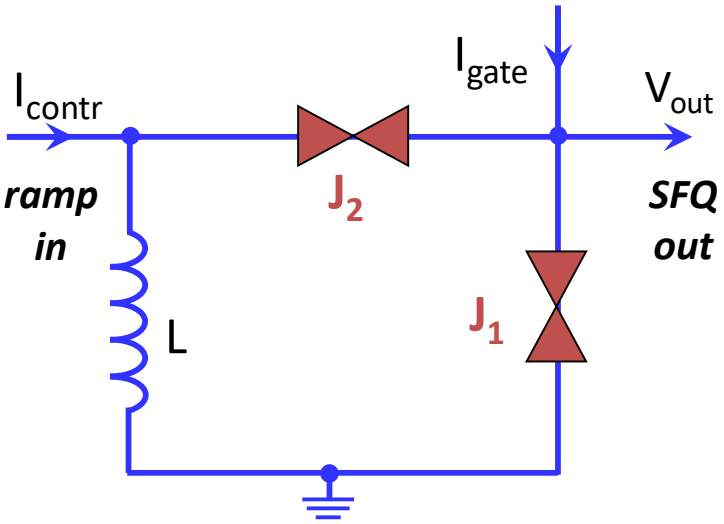
→ Nb JJ intrinsically underdamped → Shunt resitance → Pulses longer & less high

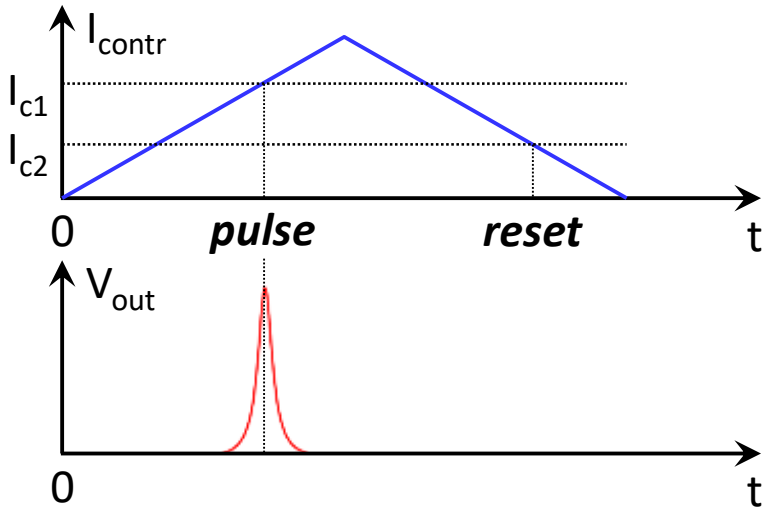
→ Single pulse with few-ps control pulse → Demanding

No control pulse → RSFQ pulse train → Natural clock

5.3.1 Basic Components of RSFQ Circuits

Generation of RSFQ pulses – rf SQUID





Replace overdamped JJ by rf SQUID with $3 \lesssim \beta_{L,\mathrm{rf}} \lesssim 10$

→ Hysteretic behavior

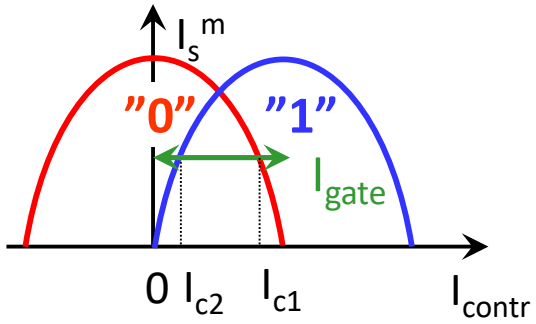
→ $0 \rightarrow 1$-transition at $I_{\mathrm{contr}} = I_1$

→ $1 \rightarrow 0$-transition at $I_{\mathrm{contr}} = I_2$

RSFQ pulse again generated with dc current pulse

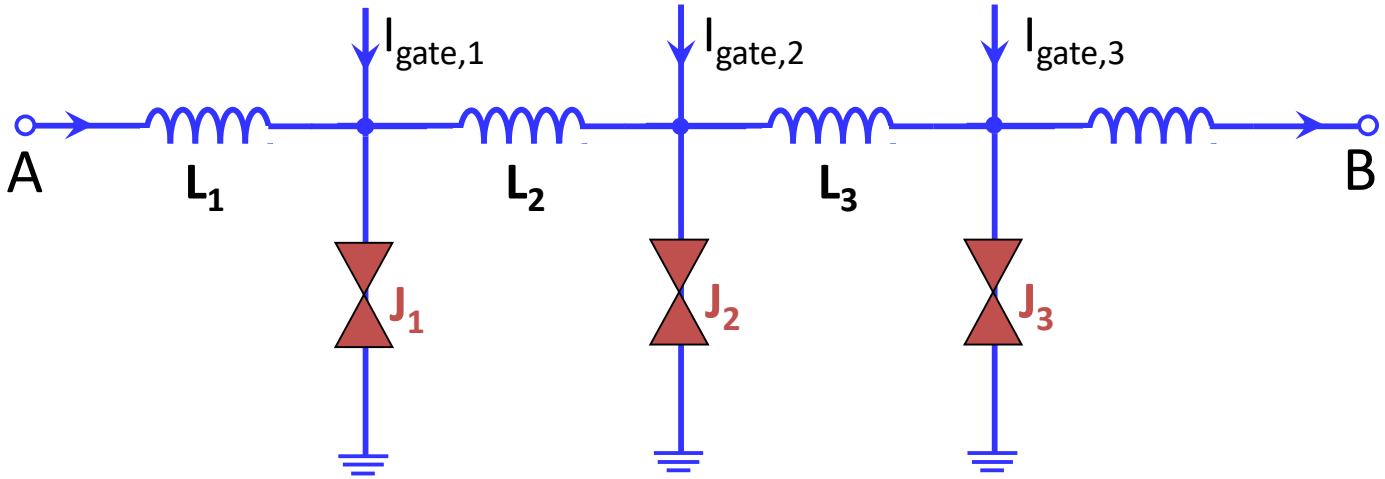
Pulse can be longer at cost of decreased amplitude

Pulse train can be generated with external RF clock



5.3.1 Basic Components of RSFQ Circuits

Josephson transmission line (JTL)



Reciprocal device

Exactly 1 fluxon localized at sinlge junction → $L_n \simeq \Phi_0/I_c$

SFQ pulse incident at A

→ Trigger consecutive 2π phase jumps in junctions

→ Fluxon propagates towards B

5 ps-pulse & 1 cm line length → No noticable attenuation

Amplification

→ $I_{c,n}$ should grow & $I_{c,n}$ decrease accordingly in propagation direction

5.3.1 Basic Components of RSFQ Circuits

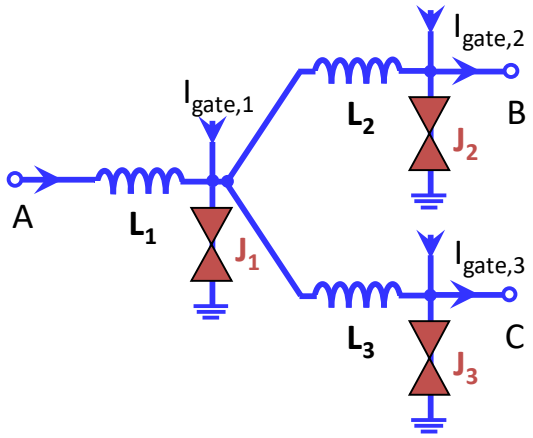
Pulse splitter

Reciprocal device

→ Symmetric with repsect to all three ports

Evident generalization of JTL

Reproduction capability used



Buffer stage

Provides isolation

J_1 and J_2 dc-biased below their critical currents $I_{c1} < I_{c2}$

SFQ pulse incident on port A

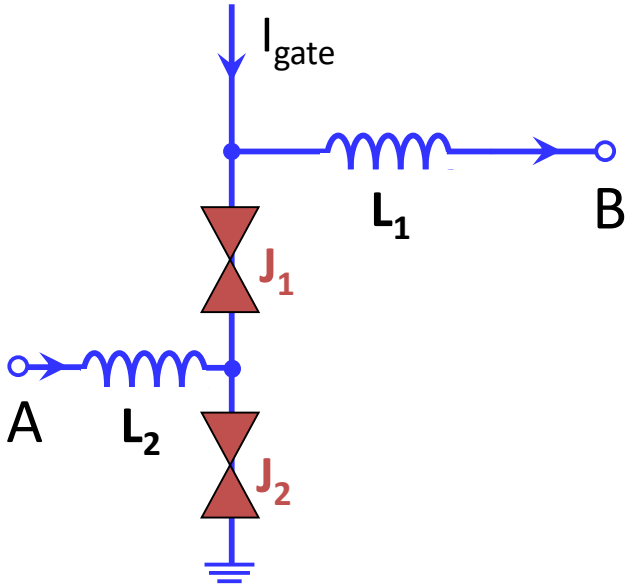
→ 2π phase shift at J_2

→ SFQ pulse output at B

SFQ pulse incident on port B

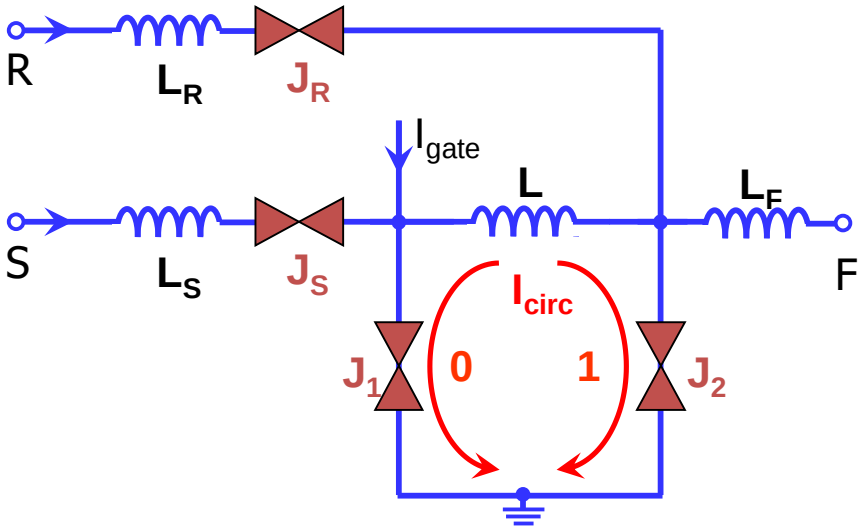
→ 2π phase shift at J_1

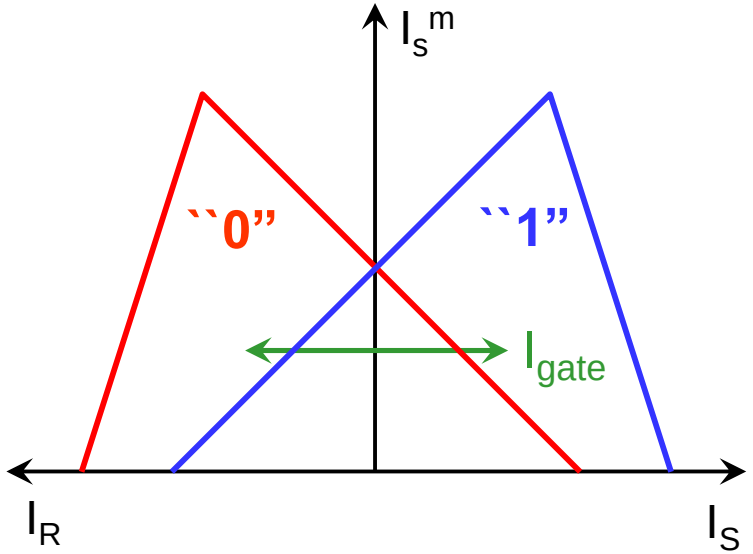
→ No output at port A



5.3.1 Basic Components of RSFQ Circuits

SFQ Memory cell: RS flip-flop register (DRO register)





Dc SQUID with $\beta_L \simeq 3$ and two JJ-buffered input lines

Information stored as quantized flux trapped inside the loop

Proper parameters and bias

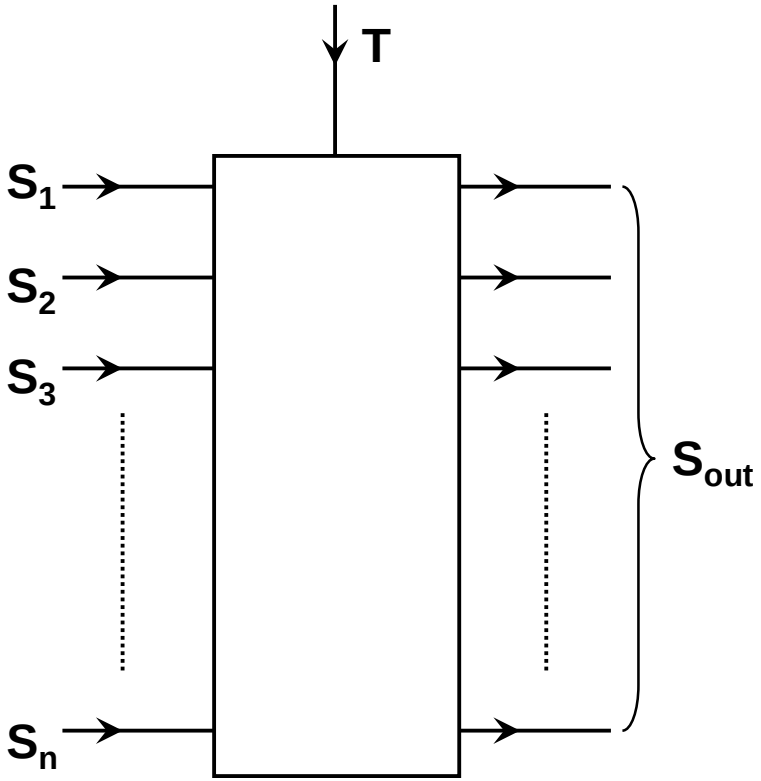
- → Incoming SFQ pulse at port S (set) triggers flux trapping („$0 \rightarrow 1$"-transition)
- → Incoming SFQ pulse at port R triggers reset („$1 \rightarrow 0$"-transition)
- → J_R and J_S protect input from setting(resetting) a 1(0) state
- → During reset, a readout pulse is emitted at port F

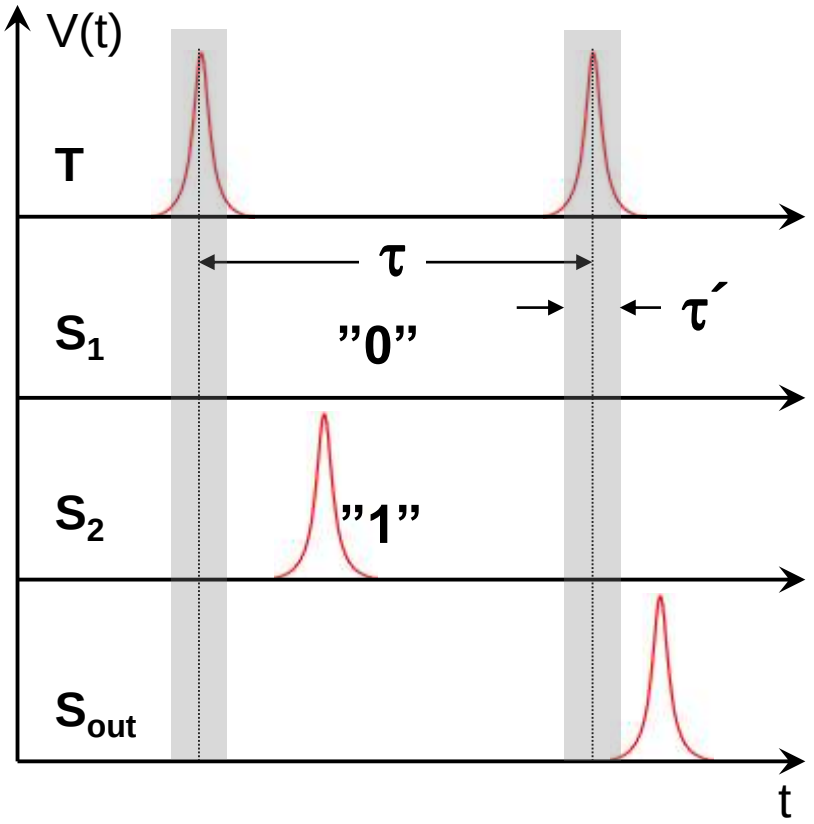
Operating principle similar to latching (flipflop) logic

High-density RAM possible, but not implemented yet (effort, resources)

5.3.2 Information in RSFQ Logic

Concept of elementary cells or timed gates (Likharev)





Each cell → Two or more stable flux states & signal RSFQ pulses S_1, S_2, …

Clock generates additional timing line T

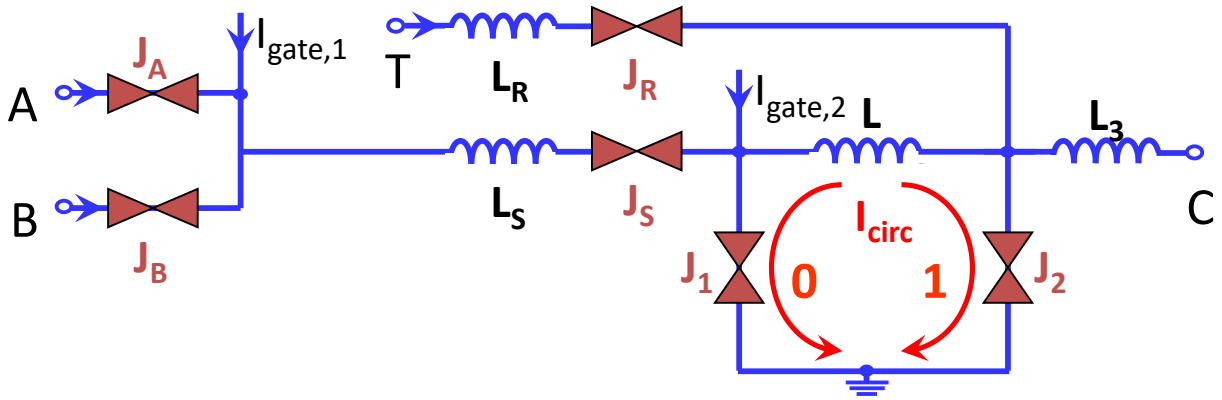
→ Sets cell to initial state „1“ at the beginning of every clock period

→ Possibly generates output pulse S_{out} at the end of every clock period

Logical „0“ and „1“ → Absence and presence of RSFQ pulse during time τ in line S_i

5.3.3 Basic Logic Gates

RSFQ OR gate



Confluence buffer connected to RS flip-flop

Initial clock pulse resets the memory to 0

One SFQ pulse enters either A or B → memory cell switches to in state 1

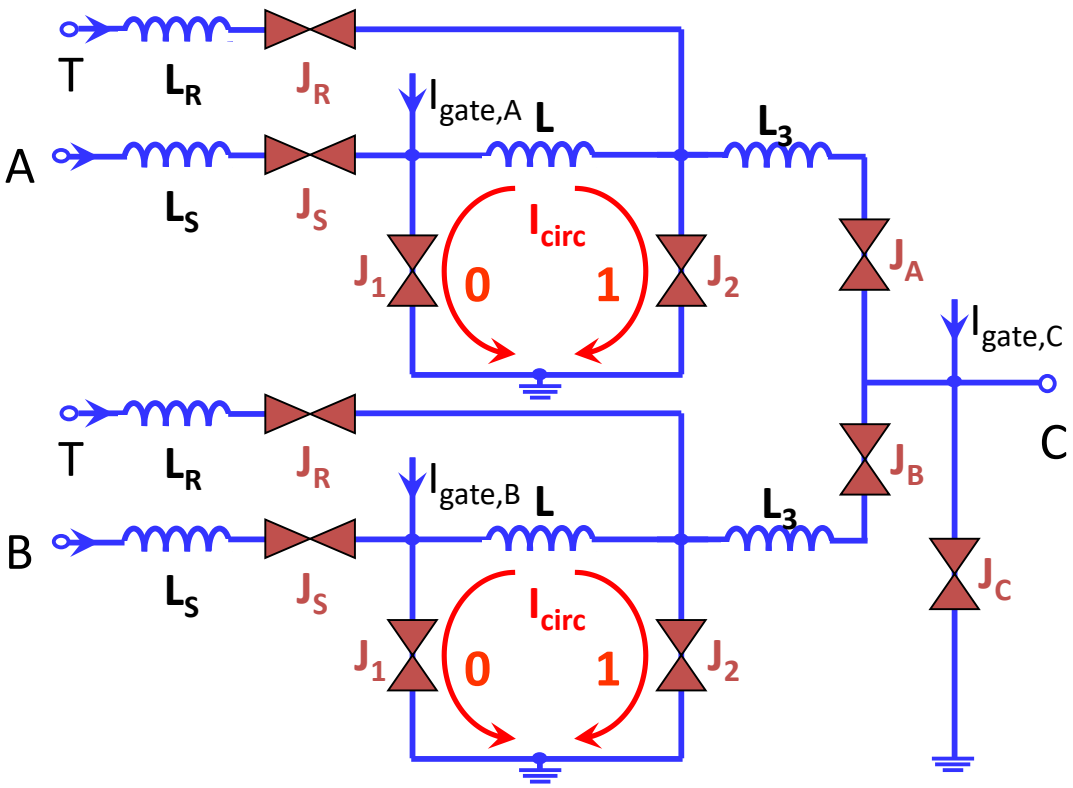
Pulses in A and B → First pulse switches memory to 1, second pulse does nothing

Clock pulse at the end → Resets memory and generates output pulse if in state 1

5.3.3 Basic Logic Gates

RSFQ AND gate

Two RS flip-flops at the inputs of a confluence buffer



Initial clock pulse resets the memories to 0

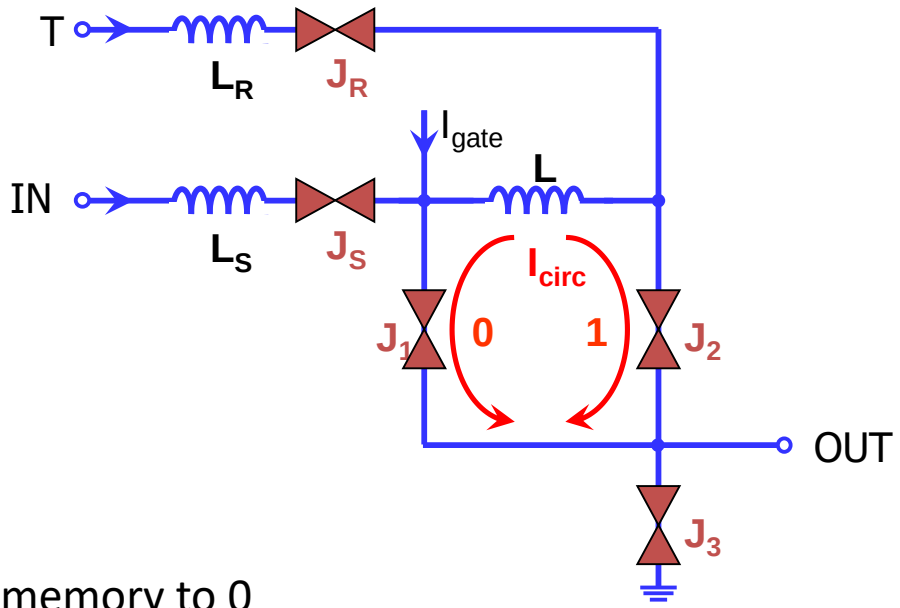
If two SFQ pulse enters A or B at different times → Memory cells for storage

Next clock trigger → Reset memories and release stored pulses simultanelously

J_c switches only if two pulses add → Only then SFQ pulse released at port C

5.3.3 Basic Logic Gates

RSFQ NOT gate



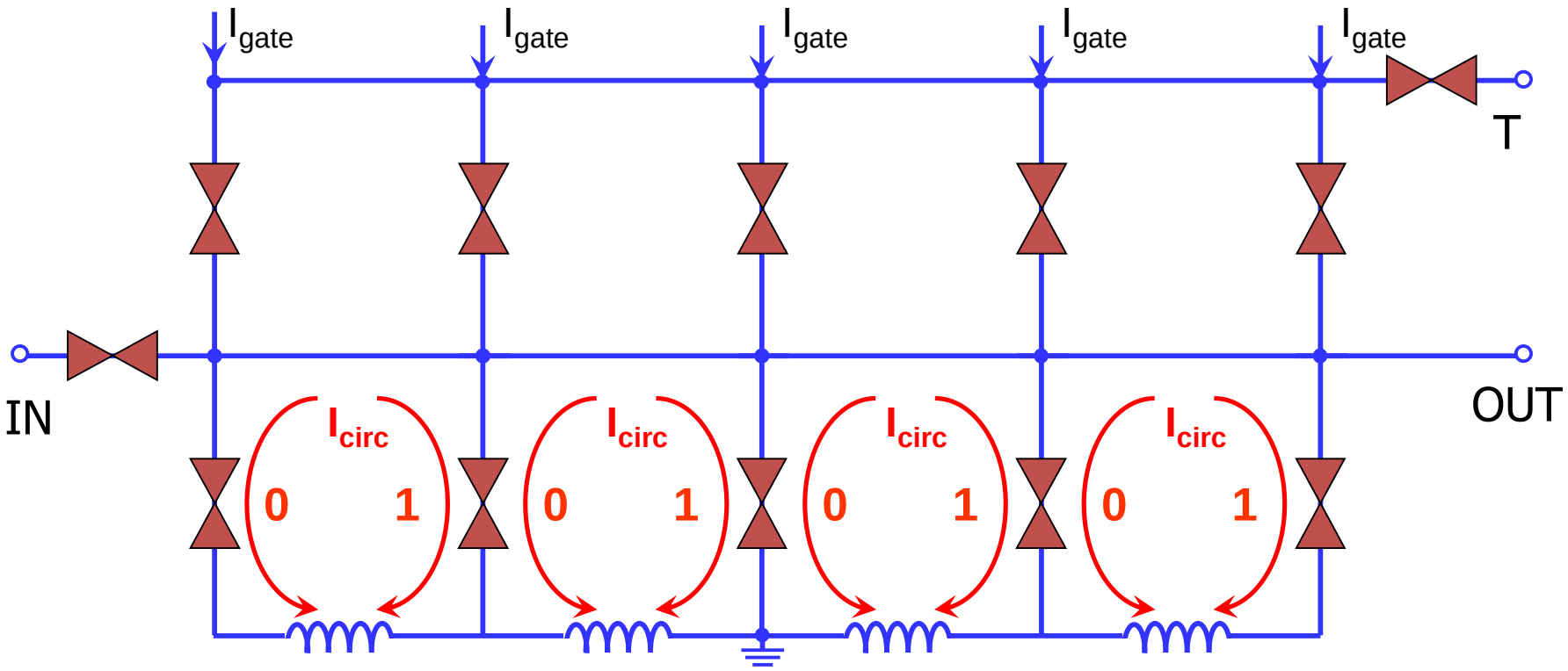
Initial clock pulse resets the memory to 0

If no pulse (state 0) enters at port IN
→ J2 carries virtually no current
→ Next trigger T pulse switches J3
→ Output of SFQ pulse (state 1)

If a pulse (state 1) enters at port IN
→ Stored in memory, increasing current through J2
→ Next trigger pulse T switches J2 and not J3
→ No output of SFQ pulse (state 0)

5.3.3 Basic Logic Gates

RSFQ shift register



Upper array acts as JTL transmittion trigger/reset pulses from port IN

First in first out (FIFO) memory

5.3.5 Maximum Speed of RSFQ Logic

Simulation → Maximum delay $\simeq 6\pi\tau_{RL}$ $\qquad \tau_{RL} = \dfrac{\Phi_0}{2\pi I_c R}$

Overdamped Josephson junctions → $\beta_C = \dfrac{2\pi}{\Phi_0} I_c R^2 C = \dfrac{2\pi}{\Phi_0} J_c R^2 C_s < 1$

for $\beta_c \approx 1$ → $\tau_{RL} = \dfrac{\Phi_0}{2\pi I_c}\sqrt{\dfrac{\Phi_0 I_c C}{2\pi}} \propto \sqrt{\dfrac{C}{I_c}}$

3 µm technology → $2\pi\tau_{RL} \simeq 3$ ps → Clock speed $\simeq 100$ GHz

Submicron technology → Clock speed $\simeq 500$ GHz

5.3.6 Power Dissipation

$$E_{\mathrm{diss}} \simeq \int I_c V dt$$

$$I_c \simeq 100\,\mu\mathrm{A} \text{ and } \int V dt = \Phi_0$$

$$\boxed{E_{\mathrm{diss}} \simeq 2 \times 10^{-19}\mathrm{J}}$$

But: power dissipation is mainly limited by dissipation in bias resistors

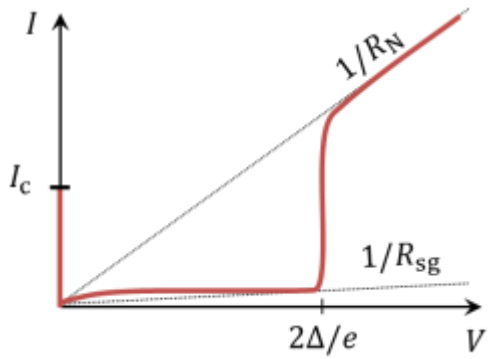
$$\rightarrow P_{\mathrm{diss}} \simeq 1\,\frac{\mu\mathrm{W}}{\mathrm{gate}}$$

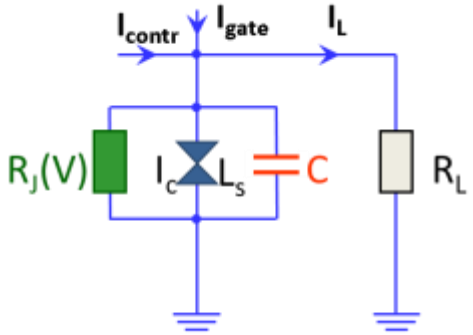
5.3.7 Prospects of RSFQ

Applications of RSFQ logic

application	no. of JJs	estimated market size
integrated SIS receivers with correlator	10^6	small
digital multichannel SQUID arrays	10^5	medium
dc voltage standards	10^4	small
ac voltage standards digital synthesizer	10^5	medium
A/D converters	10^4	large
D/A converters	10^3	medium
dc/ac quantum voltmeters	10^5	large
time-digital converters	10^3	medium
digital SFQ test circuits for rf metrology	10^3	medium
frequency dividers, digital frequency meters	500	medium
transient recorders	10^4	medium
TeraFLOP workstation	10^6	medium
PetaFLOP computer	10^9	??
Cryogenic electronics for control and readout of superconducting quantum circuits for quantum information	many	??

Summary (latching Josephson logic)





Underdamped JJ as switching gates

→ Zero and finite voltage state as 0 an 1

→ Natural emulation of semiconductior logic

$$\tau_{RC} > \tau_{LC} > \tau_{RL}$$

$$\tau_{RC} \sim 10 \text{ ps}$$

$$P_{\text{diss}} = \frac{V_g^2}{R_{sg}}$$

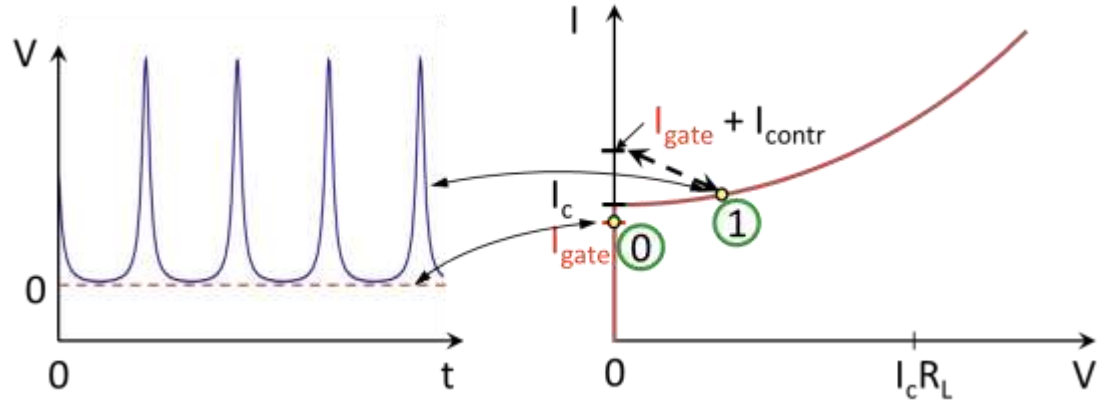
$$E = P_{\text{diss}} \cdot \tau \simeq 3 \times 10^{-18} \text{ J}$$

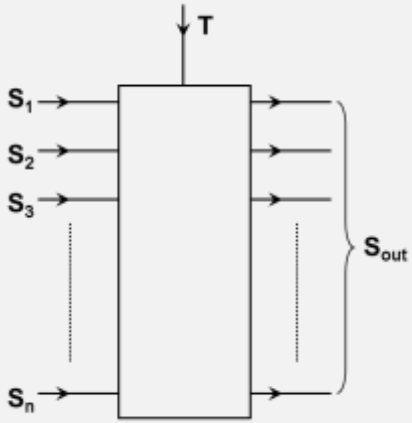
Disadvantages of Josephson logic:

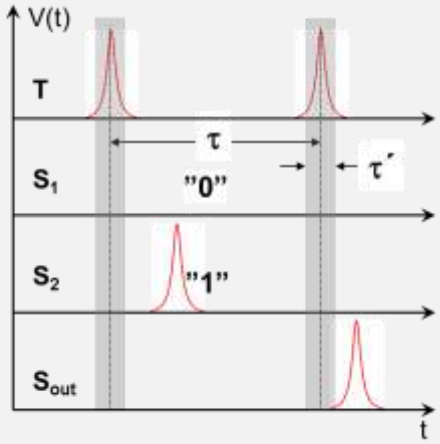
- Ac power supply and global timing required
- Speed < 1GHz due to punchthrough effect
- Switching back to zero voltage state slow (~ 1 ns)

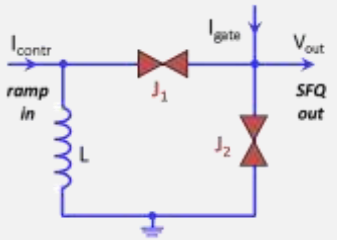
Summary (RSFQ logic)

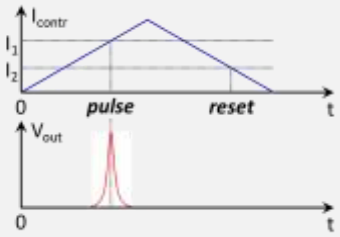
based on overdamped Josephson junctions

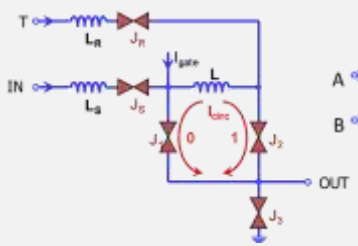


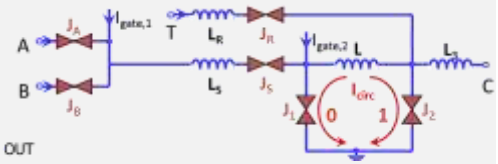












Advantages of RSFQ logic:

- typical clock frequencies above $100\ \mathrm{GHz}$
- nonlatching logic
- low power consumption $P_{\mathrm{diss}}\tau \simeq 10^{-18}\,\frac{\mathrm{J}}{\mathrm{bit}}$