# Applied Superconductivity:

## Josephson Effect and Superconducting Electronics

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# Chapter 5

# Digital Electronics

The main purpose of digital electronics is to process and store binary signals. That is, two basic elements are required for any digital computing technology: a fast switching device and a memory element for bit storage. For semiconductor digital electronics the transistor is the switch and the memory is predominantly realized by storing charge on a capacitor. In analogy, in superconducting digital electronics the Josephson junction is the switch and the memory is realized by storing magnetic flux in an inductor realized by a superconducting loop.

After addressing the basic advantages and disadvantages of superconducting devices in digital electronics in section 5.1, we discuss the foundations and technical implementation of the ***Voltage State Josephson Logic*** and the ***Rapid Single Flux Quantum Logic*** in sections 5.2 and 5.3, respectively. As an important and promising application of superconducting digital devices and circuits, in section 5.4 we discuss ***Superconducting Analog-to-Digital Converters***.

## 5.1 Superconductivity and Digital Electronics

There are only a few basic requirements for any digital technology. Firstly, the processing, which is realized by elementary logic gates, should be fast, error free and low power. Secondly, in the same way the storage of data into a memory as well as the read-out should be fast, error free and low power. Thirdly, since digital electronics requires a large number of gates and memory cells, the fabrication process of the required devices should be reproducible and cheap. Finally, it should be possible to integrate a large number of devices into a small volume. Compared to semiconductor electronics the main advantages of superconducting digital electronics are its lower power consumption and higher speed.[1] Until today, clock frequencies above 100 GHz have been realized for superconducting digital circuits.[2,3] Furthermore, the power consumption of the competing semiconductor digital electronics becomes an increasingly important problem and already today limits the further increase of clock frequency and integration level. Therefore, the main focus of digital applications of the Josephson effect is high-speed low power consumption computer systems.[4,5,6]

Today, the applications of superconducting circuits in digital electronics are still under development because the scale/amount of technology required is much larger than that of analog applications. However, superconducting digital circuit technology always has been the driving technology for other applications such as SQUIDs, mixers, etc.. The fabrication technology for high-quality, reproducible Josephson junctions with low parameter spread and the required integration technology have been developed mainly for digital applications. In turn, these technologies have greatly improved the performance of analog Josephson devices such as integrated SQUID sensors, digital-to-analog converters, etc.. Digital electronics is certainly a huge and attractive but also very competitive market. In order to make it to the market place and to compete with the established semiconductor electronics, superconducting digital electronics must show up with significant advantages over semiconducting electronics in order to compensate for several disadvantages implied by the superconducting state:

- Cooling to low temperatures is required: Since complicated integrated superconducting circuits at least at present require Nb-technology, cooling to well below the transition temperature of Nb (9.2 K) is necessary. This requires cooling by liquid helium or expensive cryocoolers. Higher operation temperatures allowing for the use of liquid nitrogen or less expensive closed cycle refrigerators would be desirable. However, up to now there is no established technology for high temperature superconductor (HTS) that would allow the reproducible fabrication of a large number of Josephson junctions and other circuit elements within the required margins of yield and parameter spread. It should be noted, however, that the disadvantage related to the required cooling of superconducting circuits becomes less severe as the competing semiconductor circuits require an increasing effort for removing the large amount of dissipated heat.

- The change-over to a new technology (e.g. from semiconductor to superconductor technology) involves huge financial investments for fabrication equipment and the development of the fabrication technology.

- New technologies for logic elements, packaging, power supply, ... have to be developed causing again significant costs.

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[3] W. Chen, V. Rylyakov, V. Patel, J.E. Lukens, K.K. Likharev, IEEE Trans. Appl. Supercond. **AS-9**, 3212 (1999).
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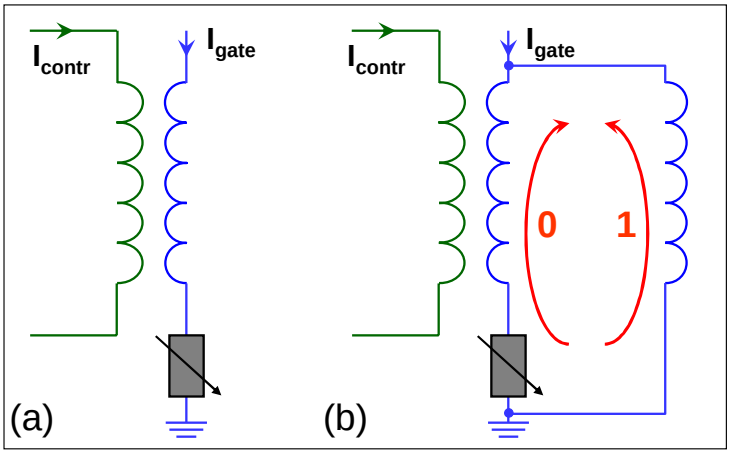


Figure 5.1: Illustration of the switching element (a) and the memory element (b) for the cryotron. The magnetic field of the control current switches the gate line into the resistive normal state represented in the equivalent circuit by the switchable series resistor.

### 5.1.1 Historical development

In this subsection we briefly address the historical development of superconducting digital circuits. Many ideas are quite old and never made it to the market place due to the dominating semiconductor technology.

1. ***Cryotron*** (1956):

   In 1956 the ***cryotron*** was suggested.[7] Here, the transition between the superconducting and normal state in a superconducting thin film was used for switching a current path. As shown in Fig. 5.1, the cryotron consists of two superconducting lines, where the control line has a higher critical magnetic field $H_c$ than the gate line. This can be realized by using different materials. The control current generates a magnetic field that exceeds $H_c$ of the gate line driving it into the normal state. With appropriate design parameters this normal gate can switch enough current to control another gate. Combining these cryotrons various logic gates can be realized. The memory cell was essentially a closed superconducting loop that could store magnetic flux of either sign (corresponding to 0 or 1) by a persistent current circulating in opposite directions. If part of the loop is also a cryotron gate, flux can be transferred into or out of the loop by driving this part into the normal state with the control current. This allows to write in or read out the stored bit.

   The major drawback of this device was the low switching speed of $\sim 10$ ns limited by the $L/R$ time. Furthermore, local self-heating in the normal state resulted in an increased time for the return into the superconducting state. Already in the early 1960s it was clear that this technology could not compete with the upcoming semiconductor integrated circuits.

2. ***Josephson Switching Device*** (1966):

   **J. Matisoo** of IBM realized the first Josephson switching device in 1966 with sub-nanosecond switching speed soon after the Josephson effect has been discovered.[8] As shown in Fig. 5.2, in this ***Josephson cryotron*** the critical current of a Josephson junction was suppressed by a magnetic field that was typically orders of magnitude smaller than the critical field of a superconductor. An even much smaller field is required to suppress the critical current of a dc SQUID. Hence, much smaller control currents and smaller inductances were required to drive the Josephson junction or

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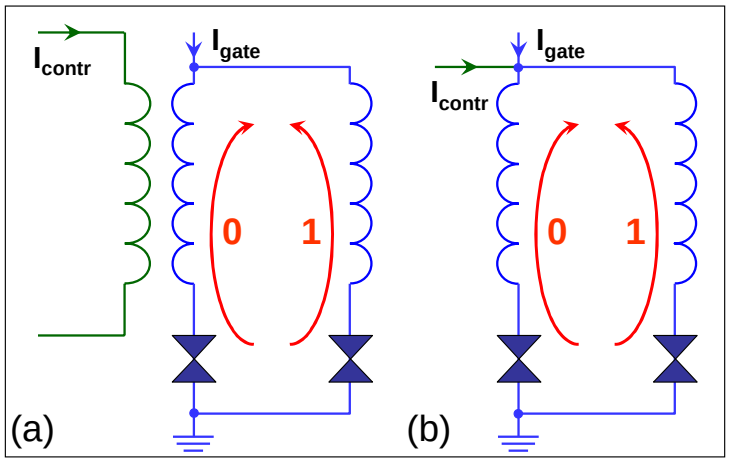


Figure 5.2: Schematic illustration of the Josephson cryotron switching and memory element. (a) Inductively and (b) directly coupled switching or memory element. The Josephson element acts as the switchable resistor.

the SQUID into the resistive state. This resulted in smaller $L/R$ and in turn shorter switching times. A loop containing Josephson junctions also could be used to store magnetic flux via a circulating current. The flux is entering and leaving the loop via one of the Josephson junctions. The more sensitive control permits the use of the natural binary bit of a superconducting loop, namely the flux quantum $\Phi_0$. The proper choice of the circuit parameters allows to switch the SQUID between zero and a single flux quantum in the loop. Of course, the large sensitivity to even small magnetic fields created also the problem that ambient magnetic fields lead to the presence of accidentally trapped magnetic flux in the circuit. This requires very good magnetic shielding by e.g. several $\mu$-metal shields. In addition, thin film Josephson circuits have been fabricated with so called magnetic moats, slots in the superconducting ground plane of the circuit, where any residual magnetic flux was trapped away from the sensitive parts of the circuit.[9]

Following the initial work on the Josephson cryotron IBM conducted a large program for developing a Josephson computer.[10] This program was stopped in 1983. In the course of this program essential computer components including logic and memory circuits and systems have been developed as well as fabrication and packaging technologies. There were two major reasons why IBM stopped the project. Firstly, the use of Pb-alloy technology did not allow to fabricate Josephson junctions with a sufficiently small spread of the critical current. Furthermore, the Pb-alloy junctions were not stable enough to withstand repeated thermal cycling. Secondly, the IBM program was focusing on latching logic gates based on underdamped Josephson junctions. This latching logic, where the current bias has to be switched off to return to the zero voltage state, has several disadvantages discussed below and did not allow for clock speeds well above 1 GHz. The former problem nowadays has been solved through the Nb-technology, the latter by using the non-latching ***Rapid Single Flux Quantum (RSFQ)*** logic.

Stimulated by the IBM activities, major Japanese computer companies and government agencies (ETL, NEC, Hitachi, Fujitsu, NTT) started the ***Japanese High Speed Computer project*** in 1981, in which the Josephson junction device was selected as one possible candidate (together with GaAs and HEMT) for the realization of future high-speed computer systems. These efforts continued even after the IBM project has been stopped and led to much progress in junction fabrication

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[10] W. Anacker, *Josephson Computer Technology*, IBM J. Res. Develop. **24**, 107 (1980).

and integration technology, device concepts and systems.[11,12,13,14] With respect to technology the most important progress was the fabrication of $Nb/Al_2O_3/Nb$ tunnel junctions instead of Pb-alloy junctions.[15] These so-called "refractory" junctions even allow the construction of circuits with large scale integration (LSI) complexity. The Nb-technology also had a large impact on the further development of other Josephson applications (sensors, mixer, AD converter, ...).

3. ***Rapid Single Flux Quantum (RSFQ) Logic*** (1985):

After the failure of the IBM project significant progress was achieved by the suggestion of the ***RSFQ (Resistive or Rapid Single Flux Quantum) logic***.[16] In RSFQ overdamped Josephson junctions are used. In this non-latching logic information is represented in a totally different way from that used in the latching voltage logic based on underdamped Josephson junctions. If an overdamped junction is biased with a current slightly larger than the critical current, the Josephson current has the form of short pulses with the pulse duration being of the order of $\Phi_0/I_cR_N$ (compare Fig. 3.7 in section 3.3). For a typical $I_cR_N$ product of 1 mV the pulse duration is only 2 ps. During a single pulse the phase difference across the Josephson junction evolves by $2\pi$. According to the 2. Josephson equation ($\dot{\varphi}/2\pi = V/\Phi_0$) this means that the phase change results in a short voltage pulse with $\int V dt = \Phi_0$. The idea of the RSFQ logic is to use these voltage pulses for the realization of logic circuits. Following the first ideas by **Likharev**[17,18] as well as **Nakajima** and coworkers[19,20] the first logic element, a T-flip-flop, has been proposed by **Silver** in 1978.[21] Today a large variety of RSFQ circuits has been implemented[22,23] with the ultimate speed of an RSFQ device ever measured experimentally being 770 GHz.[24] Major advantages of the RSFQ logic are (i) low power consumption, (ii) intrinsic memory, and (iii) very high speed.

### 5.1.2 Advantages and Disadvantages of Josephson Switching Devices

Before discussing the foundations of latching Josephson switching gates in section 5.2 and non-latching RSFQ circuits in section 5.3, we briefly address several basic advantages and disadvantages of Josephson junction based devices compare to semiconductor devices.

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[17] K.K. Likharev, *Properties of a superconducting ring closed with a weak link as a device with several stable states*, Radio Eng. and Electron. Phys. **19**, 109-115 (1974).

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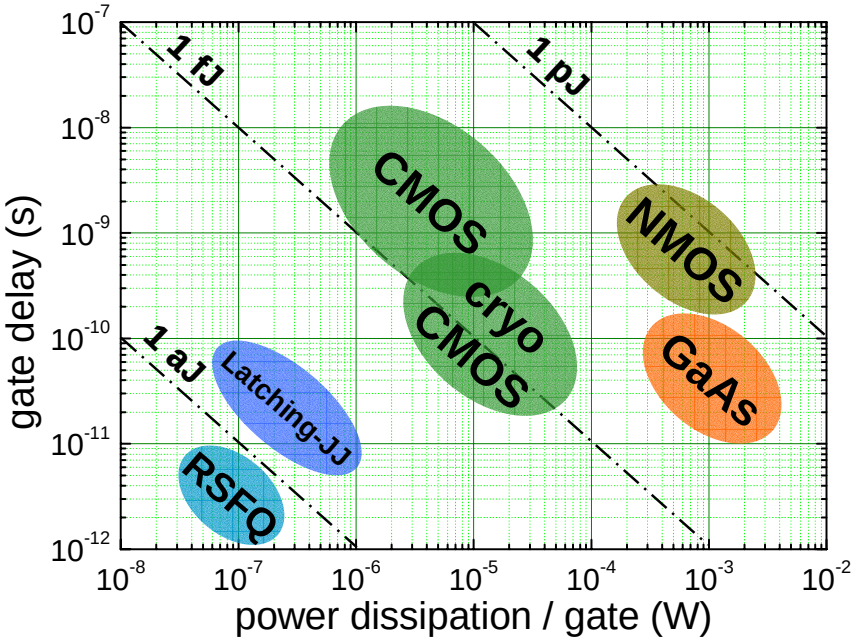


Figure 5.3: Comparison of device performance based on the delay-power relation for various devices. "Latching-JJ" stands for Josephson latching circuits, "RSFQ" represents RSFQ-based gates. Josephson devices are superior in both propagation delay and power dissipation to any semiconducting device.

**Pros:**

- Josephson junctions can switch very fast between the zero voltage and the voltage state with low power dissipation. In Fig. 5.3 the delay-power characteristics of Josephson devices are compared with various semiconductor devices. The switching delay times of Josephson devices are scattered below 10 ps, what is about one order of magnitude shorter than for semiconductor devices.

- The power dissipation per gate is $P_{\rm diss} \sim V^2/R_N$ with $V = \max[I_c R_N, \hbar\omega_p/e]$ and typically ranges between 0.1 and 1 $\mu$W (see section 5.2.2). This is by two to three orders of magnitude less than for semiconductor devices. Low power dissipation is crucial for large scale integration, which in turn is important for reducing the wiring length and thus reducing the gate delay times. The dissipated energy per gate cycle is typically in the range of $10^{-18} - 10^{-17}$ J and hence by several orders of magnitude lower than for semiconductor devices.

  In the following table we show the product $P_{\rm diss} \cdot \tau$ of the power dissipation per gate and the gate delay for a logic circuit consisting of $10^6$ switching elements. For a Josephson logic circuit the energy dissipation is only $\sim 10^6 \times 10^{-18} = 1$ pJ resulting in a power dissipation of 1 mW and 1 W for a single user at a clock speed of 1 GHz and 1 THz, respectively. For a Si based circuit these numbers are by a factor of about 1000 larger. For $10^7$ users the power dissipation of the Si circuits would be already 10 MW and 10 GW for a clock speed of 1 GHz and 1 THz, respectively. In the latter case this would correspond to the power of several nuclear power stations. This is demonstrating the demand for low power logic circuits, if we want to further increase the computing power by either increasing the clock speed or the number of switching elements. It also should be noted that the lower power dissipation of superconducting devices is inherently related to the low temperature operation. If they could be operated at higher temperature, higher power consumption would be required to overcome the thermal noise and guarantee error free operation.

| | | 1 user | | $10^7$ users | |
|---|---|---|---|---|---|
| | | dissipated power at clock speed | | dissipated power at clock speed | |
| | $P_{\rm diss} \cdot \tau$ | 1 GHz | 1 THz | 1 GHz | 1 THz |
| Si | 1 nJ | 1 Watt | 1000 Watt | $10^7$ Watt | $10^{10}$ Watt |
| Josephson | 1 pJ | 1 mWatt | 1 Watt | $10^4$ Watt | $10^7$ Watt |

- Superconducting matched striplines can be used for wiring chips and packaging. These transmission lines are capable of transferring picosecond waveforms up to frequencies corresponding to the gap energy $\omega \sim 2\Delta/\hbar$ over virtually any interchip distance with a speed approaching that of light, and low attenuation and dispersion.[25,26,27] The wave impedance $Z$ of a microstrip line is given by (cf. section 8.1)

$$Z\,[\Omega] \;=\; 60\,\frac{\sqrt{t_I t_M}}{W\sqrt{\varepsilon}}\;, \qquad t_M \;=\; t_I + 2{\rm Re}\delta \tag{5.1.1}$$

  and can readily be made close to the Josephson junction resistance (which is of the order of its normal resistance). With a typical width $W \simeq 1\,\mu$m and an insulator thickness $t_I \simeq 0.3\,\mu$m a value $Z \simeq 10\,\Omega$ can be realized. The character of signal propagation in these lines is ballistic rather than diffusive and the contribution $\tau_i$ to the delay per gate is quite small (typically $\tau_i \simeq 10$ ps for lines as long as 1 mm). The absence of notable dispersion up to frequencies of $10^{12}$ Hz makes them the only means to transfer ps-pulses along a chip. It is also very important that these lines can be quite densely laid out (since spacing between the lines and their width are limited only by the available patterning technology), while having low crosstalk.

- Refractory Josephson junctions can nowadays be fabricated reproducibly with small parameter spread using the Nb technology.

**Cons:**

- At present there are no feasible transistor-like three-terminal devices with high gain such as semiconductor transistors. This causes problems to realize a high fan-out, the ability of a single logic gate to trigger a large number of consecutive gates.

- Due to the lack of transistor like devices providing gain, integrated Josephson electronic circuits usually require a small parameter spread of the Josephson junctions.

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## 5.2 Voltage State Josephson Logic

In this section we discuss the use of underdamped Josephson junctions as switching gates in a voltage state Josephson logic. As already discussed in chapter 3, for current values ranging between the critical current $I_c$ and the return current $I_R$ there are two possible voltage states, namely the zero and finite voltage state. These states can be assigned to the logical states “0" and “1". Voltage-state logic is a natural emulation of semiconductor technology in that data is encoded by steady voltage levels. This is a very significant advantage. Since Josephson junction voltage-state logic resembles semiconductor logic, the entire and elaborate edifice of digital circuit design tools and concepts used for semiconductor integrated circuits can be rather directly applied to develop superconducting circuits. The design infrastructure for the RSFQ logic discussed in 5.3 is much less well-developed, although the semiconductor experience is still highly relevant.

### 5.2.1 Operation Principle and Switching Times

Fig. 5.4 illustrates the switching of an underdamped Josephson junction from the “0” ($V = 0$) state along the load line to the “1” ($V = V_g$) state. The load line is defined by the load resistance $R_L$. Initially, the junction is biased with a current $I_{\rm gate} < I_c$. If an input current $I_{\rm contr}$ is added to $I_{\rm gate}$ so that $I_{\rm contr} + I_{\rm gate}$ exceeds $I_c$, the junction switches into the voltage state. The load resistor $R_L$ is chosen to be much smaller than the sub-gap resistance $R_{\rm sg}$ of the junction. Therefore, almost all of the current through the junction is transferred to the load after the junction switches.

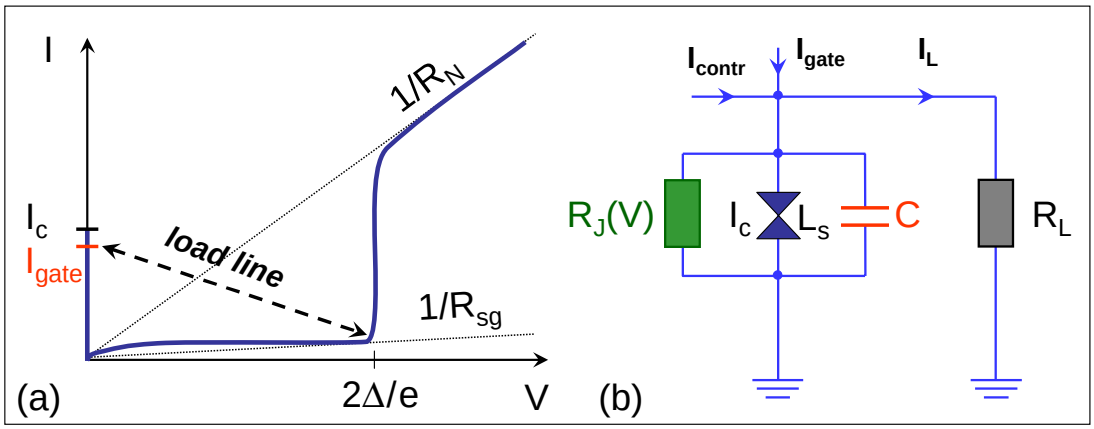


Figure 5.4: (a) Schematic illustration of the switching process of a Josephson tunnel junction along the load line. (b) Equivalent circuit for the Josephson junction switching device. The Josephson junction is represented by an ideal junction with critical current $I_c$ and kinetic Josephson inductance $L_s$, which is shunted by the junction capacitance $C$ and the voltage dependent normal resistance $R_J(V)$. The switching is along the dashed line defined by the load resistance $R_L$.

As shown by the equivalent circuit for the Josephson junction switch in Fig. 5.4b the Josephson element can be replaced by the Josephson inductance (compare section 2.1.4)

$$L_s = \frac{\Phi_0}{2\pi I_c \cos\varphi(t)} = \frac{L_c}{\cos\varphi(t)} \qquad \text{with} \qquad L_c = \frac{\Phi_0}{2\pi I_c} = \frac{\hbar}{2eI_c}\,, \tag{5.2.1}$$

which is shunted by a capacitance $C$ and a voltage dependent resistance $R_J(V)$.

### Characteristic Time Scales

In order to estimate the characteristic times we consider the equivalent circuit of the Josephson junction switch in Fig. 5.4b. Due to the nonlinearity of the Josephson junction ($L_s = L_c/\cos\varphi$, $R_J = R_J(V)$) we have to deal with a nonlinear *LCR* circuit with the total *R* given by the parallel connection of the junction resistance $R_J$ and the load resistance $R_L$. For getting rough estimates we can approximate the circuit by a linear *LCR* oscillator by simply replacing $L_s$ by $L_c$ and $1/R(V) = 1/R_L + 1/R_J(V)$ by either $1/R_L + 1/R_{\rm sg}$ or $1/R_L + 1/R_N$ depending on whether $V < 2\Delta/e$ or for $V > 2\Delta/e$. Considering the switching process of the Josephson junction device we then have to consider the following three characteristic time constants (compare sections 3.1.1 and 3.1.2):

$$\tau_{RC} = RC \tag{5.2.2}$$

$$\tau_{RL} = \frac{L_c}{R} = \frac{\Phi_0}{2\pi I_c R} \tag{5.2.3}$$

$$\tau_{LC} = \sqrt{L_c C} = \sqrt{\tau_{RC}\tau_{RL}} = \left(\frac{\phi_0 C}{2\pi I_c}\right)^{1/2} \tag{5.2.4}$$

It is expected that the switching speed of the Josephson junction is limited by the slower of the time constants $\tau_{RC}$ and $\tau_{RL}$. The time constant $\tau_{LC}$ is the geometric mean of these two time constants and therefore always ranges between them. Since we are considering underdamped Josephson junctions with hysteretic IVCs, the McCumber parameter must satisfy $\beta_C = \tau_{RC}/\tau_{RL} > 1$. Therefore, the time constants order as

$$\tau_{RC} > \tau_{LC} > \tau_{RL} \tag{5.2.5}$$

and the switching time is expected to be limited by $\tau_{RC} = RC$. Note that $1/R = 1/R_L + R_{\rm sg}$ for $V < 2\Delta/e$ and $1/R = 1/R_L + 1/R_N$ for $V > 2\Delta/e$ resulting in different time constants $\tau_{RC}$ and $\tau_{RL}$ in both regimes.

The switching process of a junction is shown in Fig. 5.5. The switching delay mainly consists of two components: the so-called ***turn-on*** delay $\tau_t$, which is required to increase the junction current from $I_{\rm gate} < I_c$ to $I_c$, and the ***rise-time*** $\tau_r$, which is required to increase the junction voltage after exceeding $I_c$ to about the gap voltage $V_g = 2\Delta/e$. The latter is mainly the time required for charging the junction capacitance.

### Turn-on Delay $\tau_t$

In order to switch the junction we have to increase the junction current from $I_{\rm gate} < I_c$ by $\Delta I$ so that $I_{\rm gate} + \Delta I > I_c$. Initially, this current is not flowing through the junction (due to its kinetic inductance $L_c$) but through the capacitance *C* and the resistance *R*. Therefore, $\tau_t$ is the characteristic time required for redirecting this current through the junction. It is given by

$$\tau_t = \sqrt{\frac{\Phi_0}{2\pi}\frac{C}{\Delta I}} = \tau_{LC}\sqrt{\frac{I_c}{\Delta I}} \tag{5.2.6}$$

We see that $\tau_t$ is proportional to $\sqrt{C}/\sqrt{\Delta I}$. Therefore a small junction capacitance and a high overdrive current $\Delta I$ decrease $\tau_t$.

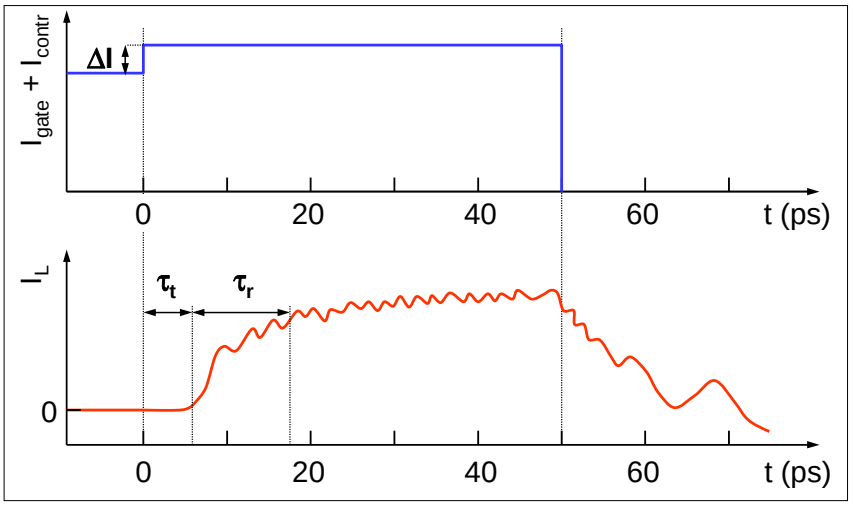


Figure 5.5: Output current waveform $I_L(t)$ when the junction switches to the voltage state. The total switching delay is composed of two components: turn-on delay $\tau_t$ and rise time $\tau_r$. The data are obtained with a computer simulation for a junction with critical current $I_c = 100\,\mu$A, a sub-gap resistance $R_{sg} = 150\,\Omega$, normal resistance $R_N = 15\,\Omega$, capacitance $C = 1$ pF, and load resistance $R_L = 10\,\Omega$. The bias current is stepped from $I_c$ to $I_c + \Delta I = 1.1 \cdot I_c$.

**Rise Time $\tau_r$:**

The rise time is the time required to charge the junction capacitance. It is given by[28]

$$\tau_r \quad = \quad RC \ , \tag{5.2.7}$$

where $R$ is the total resistance given by $1/R = 1/R_J(V) + 1/R_L$. In order to transfer a large current to the load, $R_L$ is usually chosen much smaller than the junction sub-gap resistance, so that $\tau_r = R_L C$. Furthermore, $R_L$ is chosen that $I_c R_L \simeq V_g = 2\Delta/e$ in order to make use of the maximum voltage swing (see Fig. 5.4a). Then, the rise time can be written as

$$\tau_r \quad = \quad R_L C \ = \ \frac{2\Delta\, C}{e I_c} \ . \tag{5.2.8}$$

Fig. 5.5 shows a characteristic switching waveform obtained by computer simulation.

Typical values for Nb junctions are $J_c = 10^3$ A/cm$^2$, $C/A \simeq 5\,\mu$F/cm$^2$, $\Delta I/I_c \simeq 0.1$, and $2\Delta/e \simeq 3$ mV. This results in $\tau_t \simeq 4$ ps and $\tau_r \simeq 10$ ps comparable to the simulation results in Fig. 5.5. The total delay for Nb Josephson switching devices would then typically be $\tau = \tau_t + \tau_r \simeq 14$ ps. Both $\tau_t$ and $\tau_r$ depend on the ratio $C_s/J_c$ of the specific junction capacitance, $C_s = C/A$, and the critical current density, $J_c = I_c/A$. Smaller delay times and faster switching can therefore be obtained by reducing this ratio, i.e., by increasing the plasma frequency $\omega_p = \sqrt{2eJ_c/\hbar C_s}$. This can be achieved by reducing the thickness $t_I$ of the tunneling barrier. Although the specific junction capacitance increases proportional to $1/t_I$, this is by far overcompensated by the exponential increase of the critical current density.

We note, however, that on increasing $J_c$ we are at the same time decreasing the resistance times area product $\rho_N = R_N A$, since $J_c \rho_N \sim 2\Delta/e$ stays about constant for superconducting tunnel junctions. Then, we are also decreasing $\beta_C \propto J_c \rho_N^2 C_s$ and we are finally entering the overdamped case. However, for

[28] Note that for overdamped junctions with $\beta_C < 1$ the smallest time constant is $\tau_{RL}$ and the rise time is determined by $\tau_r = L_c/R_L = e\Phi_0/4\pi\Delta$.

$\beta_C < 1$ the switching speed is determined by $\tau_{RL}$, which is now the largest time constant. For $\beta_C = 1$ all characteristic times $\tau_{RL}$, $\tau_{RC}$ and $\tau_{LC}$ are the same. It is easy to show that in this case the switching speed, which is set by the larger of $\tau_{RL}$ and $\tau_{RC}$ is minimum.

#### Steering time

The steering time $\tau_{st}$ is required to redistribute the current in a circuit with an inductance $L$. With the typical voltage scale given by $2\Delta/e$ we obtain from $V = 2\Delta/e = L\dot{I}$ with $\dot{I} = I_{\rm gate}/\tau_{st}$

$$\tau_{st} \quad = \quad \frac{LI_{\rm gate}}{2\Delta/e} \ . \tag{5.2.9}$$

Usually $LI_{\rm gate}$ is chosen to be much larger than $\Phi_0$. For $LI_{\rm gate}/\Phi_0 \sim 10$ the steering time $\tau_{st} \simeq 10\,$ps is obtained for Nb junctions.

#### Conclusions on Delay Times

Summarizing our discussion on delay times we can state the following:

- The characteristic times $\tau_t$, $\tau_r$, and $\tau_{st}$ of Josephson switching devices are of the order $\simeq 1 - 10\,$ps for Josephson junction based on Nb technology.
- Since $\tau_t \propto \sqrt{C_s/J_c}$ and $\tau_r \propto C_s/J_c$, it is advantageous to use junctions with low specific capacitance $C_s = C/A$ and high critical current density $J_c = I_c/A$, that is, with large plasma frequency $\omega_p = \sqrt{2eJ_c/\hbar C_s}$.

### 5.2.2 Power Dissipation

The power dissipated when a Josephson junction switches from the superconducting state to the voltage state as shown in Fig. 5.4 is given by

$$P_{\rm diss} \quad = \quad \frac{V_g^2}{R_{sg}} \ , \tag{5.2.10}$$

where $R_{sg}$ is the sub-gap resistance of the junction. For a Nb junction with a $R_{sg} \simeq 30\,\Omega$ one obtains $P_{\rm diss} \simeq 3 \times 10^{-7}\,$Watt, which amounts to an energy dissipation per switching cycle $E = P_{\rm diss} \cdot \tau \simeq 3 \times 10^{-18}\,$J (compare latching-JJ in Fig. 5.3). This value has to be compared to values obtained for semiconducting or expected for high-temperature superconducting (HTS) devices:

| material | $P_{\rm diss} \cdot \tau$ (Joule) |
|---|---|
| Si | $10^{-8} - 10^{-10}$ |
| GaAs | $10^{-8} - 10^{-10}$ |
| HEMT | $10^{-10} - 10^{-11}$ |
| HTS | $3 \times 10^{-15}$ |

For RSFQ logic (cf. section 5.3) $P_{\rm diss} \cdot \tau \simeq 10^{-18}$ Joule is obtained, which would yield a power dissipation per area of 1 W/cm$^2$ at an integration density of $10^7$ gates/cm$^2$. Such power density can be easily removed by liquid helium. Note that for the same integration density the power density of semiconductor circuits is by several orders of magnitude larger giving severe problems with heat removal.

At a typical operation temperature $T/T_c \simeq 0.5$ of Josephson junction circuits the sub-gap resistance is determined by thermally activated quasiparticles resulting in $R_{sg} \simeq 10R_n$. The device application determines the minimum critical current $I_c^{th}$, which is needed for a reliable device operation[29]. Since the $I_cR_n$ product for SIS junction is a material parameter with $I_cR_n \simeq \Delta/e = V_g$, we obtain

$$R_{sg}^{th} \lesssim \frac{V_g}{I_c^{th}} \times 10 \simeq 30\,\Omega \tag{5.2.11}$$

for $T = 4.2$ K, $I_c^{th} = 100\,\mu$A, and $V_g = 3$ mV.

### 5.2.3 Switching Dynamics, Global Clock and Punchthrough

#### Switching Dynamics

The switching dynamics of Josephson junction digital circuits strongly depends on whether the junctions are under- or overdamped. For the voltage state Josephson logic underdamped junctions are required, whereas for the RSFQ logic discussed below overdamped junctions are used. Let us first discuss the switching behavior of an underdamped junction with $\beta_C \gg 1$. The IVC of such a junction is strongly hysteretic. The switching behavior can be discussed qualitatively by considering Fig. 5.5. If the bias current is increased from $I < I_c$ to $I > I_c$ (or equivalently if the critical current is suppressed below $I_{\rm gate}$) the junction switches into the resistive state and the current is redirected to the load resistance $R_L$. The junction voltage is obtained by multiplying the current $I_L$ shown in Fig. 5.5 by the load resistor $R_L$. It is obvious that due to its hysteretic IVC the junction latches into the voltage state. The rise time of the junction voltage is determined by the *RC* time constant as discussed above. Furthermore, the junction voltage shows small (plasma) oscillations typical for the underdamped limit with the oscillation period given by $2\pi\tau_{LC}$ (about 2 ps in Fig. 5.5). In order to reset the junction to the zero voltage state, the current has to be switched off. The junction then returns to the zero voltage state with the time constant given by $\tau_{RC}$. Due to the underdamping the decay of the junction voltage is not smooth but accompanied by characteristic oscillations.

#### Global Clock

In order to operate a latching voltage state Josephson logic circuit the bias current has to be switched on and off periodically. The rf-power required per gate is well beyond that which can be produced by a similar gate. Thus, the clock signals must be generated externally, so that the latching circuits are restricted to external (global) timing. Obviously, the use of a global clock system, where the power is cycled on and off once each cycle, is an adequate choice for a latching logic Josephson circuit.[30] In a complex circuit with a large number of junctions the current bias could be distributed to the junctions in parallel using a voltage bias and a resistor network. In any case the development of a power supply operating in the GHz regime is a technical challenge. In particular, the rf-currents necessary to drive

[29] $I_c^{th}$ is given by the requirement that thermally induced switching to the voltage state should be negligibly small (compare section 3.4).

[30] S. Hasuo, T. Imamura, Proc. IEEE **77**, 1177 (1989).

a VLSI circuit would be very high and cause considerable crosstalk. Note that the requirement of an ac-power supply is completely different to semiconductor technology, where a dc-power supply is used.

Of course, an implicit requirement of a global biasing scheme is that the output value of a given gate is stored during the off time. This requires a latch between each gate, where the latch accepts the data during the turn-off period and transmits it again during the next turn-on. The latch may be based on a persistent current in a SQUID loop. The loop can store a binary bit even in the absence of the bias current.

Two different types of power supplies have been suggested: (i) a single-phase bipolar power system[31] and (ii) a 2- or 3-phase unipolar power system. For the single-phase system, logical operations are performed on both the positive and negative portion of the power current and the transition period between the positive and negative branch is used to reset the gates. However, for this operation the so-called punchthrough phenomenon discussed below is a serious problem and limits the clock frequency. The multiphase power supply has the advantage that it does not require a latch, since the data can be read out to the next circuit operated by the next phase power cycle.

### Punchthrough

For any global clock system the goal is to run the systems at the highest possible clock frequency. This however means that we have to consider an underdamped Josephson junction with a time-varying current source. As we have seen in section 3.3 this results in current steps in the IVC at constant voltages $V_n = n \cdot \Phi_0 f_1$, where $f_1$ is the frequency of the ac current source and $n$ an integer. These current steps can even cross the current axis (zero current steps) and are used for the Josephson voltage standard (see chapter 6). Therefore, upon switching off the bias current, the junction cannot only return to the zero voltage state but also to one of the voltages $V_n$ of the current-axis crossing current steps. Furthermore, using a bipolar power supply, the junctions may not reset to the zero voltage state during the transition from the positive to the negative branch of the cycle but switch through to the negative voltage branch. This phenomenon is known as the ***punchthrough effect***.[32,33] If one would switch on and off the power supply, the junction may return to the voltage state when the bias current is switched on again after a too short period, since it performs small plasma oscillations for a certain time after switching off the bias current.[34] The only way to avoid this problem and to guarantee save return to the zero voltage state is to reduce the clock frequency or to increase the damping. The former is reducing the performance of the digital circuit. Actually, the maximum clock frequency of Josephson voltage state logic circuits was limited to a few GHz what is much to low to compete with semiconductor circuits. The latter results in smaller $\beta_C$ and in turn larger return currents $I_R \propto I_c/\sqrt{\beta_C}$ (compare (3.3.16)). Then the junction no longer safely stays in the voltage state.

In a more general view the notation "punchthrough" has been used for the maximum speed errors of the Josephson voltage-state logic in analogy with certain errors in transistor operation. This name gives the impression that these errors are due to the device structure and hence could be eliminated with better technology. This is not correct. In fact, the errors are intrinsic since they are directly related to the topology of the phase space of a Josephson junction. As we have already seen, the fundamental parameters for the Josephson effect are the current $I$ and the phase difference $\varphi$, not $I$ and $V$. The Josephson equation $V = (\hbar/2e)\dot{\varphi}$ states that if the voltage is constant the phase is increasing rapidly, i.e. it is essentially undefined in the voltage state. The Josephson equation $I_s = I_c \sin\varphi$ on the other hand states that the phase must be well defined in the zero-voltage state. Therefore, in order to reset a

[31] H.C. Jones, T.R. Gheewala, IEEE J. Solid State Circuits **17**, 1201 (1982).
[32] R.E. Jewett, T. Van Duzer, IEEE Trans. Magn. **MAG-17**, 599 (1981).
[33] E.P. Harris, W.H. Chang, *Punchthrough in Josephson Logic Devices*, IEEE Trans. Magnetics **MAG-17**, 603 (1981).
[34] Q.P. Herr, M.J. Feldman, *Error Rate of a Superconducting Circuit*, Appl. Phys. Lett. **69**, 694 (1996).

Josephson junction from finite voltage to zero voltage ***the phase must be recaptured***. We can use this picture to calculate the minimum error rate of voltage-state logic as a function of operating speed. The conclusion is that the bit error rate due to phase recapture is too large for an integrated circuit operating at 10 GHz.

**The Pendulum Analogue:** We can intuitively understand the punchthrough phenomenon in the pendulum analogue often used in chapter 3. An underdamped junction corresponds to a pendulum with large mass and small damping. Once the pendulum is rotating (corresponding to the voltage state) it goes on to rotate for a considerable time even if the driving torque (corresponding to the applied current) is switched off and then performs oscillations around the bottom before it finally settles down. If the driving torque, i.e. the bias current, is switched on again during the oscillation period, the pendulum may start to rotate again. That is, if we do not wait for a sufficiently long period in the off state (corresponding to a decrease of the frequency of the global clock), the junction may prematurely switch into the resistive state again.

The pendulum analogue makes clear that the only way to get rid of the punchthrough effect is to increase the damping. Then, however, we can no longer use the voltage state logic requiring hysteretic IVCs with two well-defined voltage states for the same current. In general, depending on the damping we can distinguish two major classes of Josephson logic circuits. In the voltage state or latching logic based on underdamped junctions the "off-state" is the $V = 0$ state, while the "on-state" corresponds to the $V \neq 0$ state with $V \simeq 2\Delta/e$. Due to the hysteretic nature of the IVCs the junction stays in the "on-state" until it is reset (latching logic). In contrast, the flux state logic discussed in section 5.3 is based on overdamped junctions. Here, the binary logic states are realized by the rapid passage of a single flux quantum (RSFQ pulse). This represents a nonlatching logic, since the junction automatically resets into the zero voltage state. We will see that the RSFQ circuits can operate at much higher clock frequencies but require a more complicate timing associated with the motion of the RSFQ pulses.

### 5.2.4 Josephson Logic Gates

Although the voltage state Josephson logic cannot be used for ultrafast speed due to the reasons discussed above, many technical accomplishments were first demonstrated using voltage state logic. Therefore, in this section we briefly describe the key elements of voltage state logic circuits based on hysteretic junctions. The newer non-latching RSFQ logic is then discussed in section 5.3.

In order to realize logic operations various logic gates have to be designed. The general requirements for practical logic gates are:

- high ***fan out***: a single switching gate should be capable of triggering $N$ consecutive gates
- large operating margins for stable operation
- small size allowing for very large scale integration (VLSI)
- short switching time allowing for high clock frequency
- low power dissipation allowing for high integration density
- sufficient input – output isolation allowing for directionality of logic signals

Note that the Josephson switching device shown in Fig. 5.4 cannot be used in logic circuits because there is no input-output isolation. Therefore, it is very difficult to get directionality of the logic signal in the

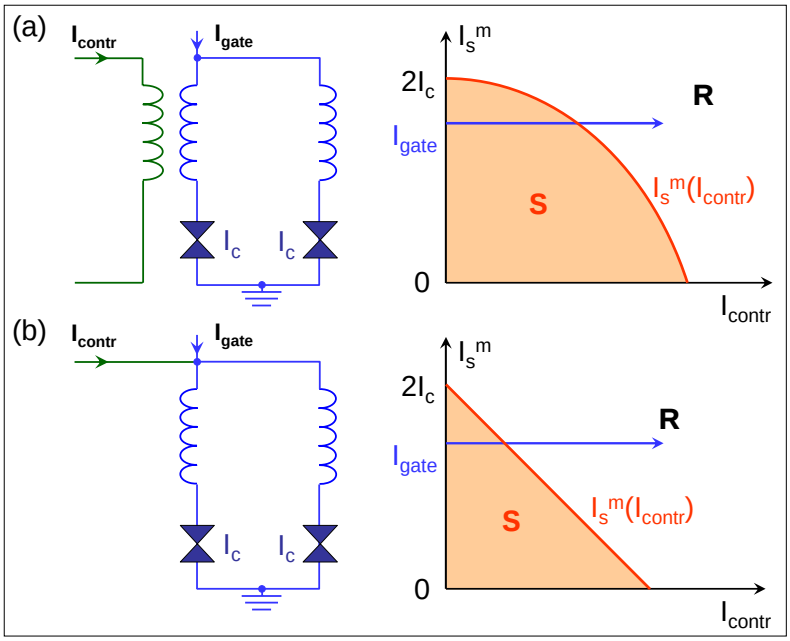


Figure 5.6: Sketch of the equivalent circuit and the threshold characteristics $I_s^m(I_{\rm contr})$ for (a) a magnetically and (b) a directly coupled gate.

circuit. It is evident that the current switched from one gate can flow in both forward and backward direction.

Until today a large number of different devices have been suggested, which can be classified into two types according to the way they are controlled: (i) magnetically coupled gates and (ii) directly coupled gates. These basic gate types together with their threshold characteristics are shown in Fig. 5.6. The threshold characteristic corresponds to the dependence of the maximum supercurrent $I_s^m$ on the control current $I_{\rm contr}$. The threshold curve $I_s^m(I_{\rm contr})$ separates the superconducting or zero voltage regime from the resistive or finite voltage regime. For the magnetically controlled gate the maximum supercurrent $I_s^m$ of a single junction or a dc-SQUID is reduced by the magnetic field generated by the control current $I_{\rm contr}$ below the applied gate current $I_{\rm gate}$ and the device switches from the superconducting (S) into the resistive (R) state. The corresponding threshold characteristics are about a Fraunhofer diffraction pattern or a $|\cos(I_{\rm contr})|$ dependence for the single junction and the dc-SQUID, respectively. For the directly coupled gate the control current is directly injected and the threshold characteristic takes the form $I_s^m = 2I_c - I_{\rm contr}$.

### Magnetically coupled gates

A typical magnetically coupled gate is the ***3-Junction Interferometer Logic (JIL) gate***,[35] which is shown in Fig. 5.7 together with its threshold characteristic. When the control current $I_{\rm contr}$ applied to the control line is large enough, the gate switches to the voltage state. Three junction SQUIDs are used because of their wider operating margins. By choosing the SQUID critical currents $I_{c1} = I_{c3} = I_{c2}/2$ the side lobes between the main lobes in the threshold characteristics are suppressed and a wider operating window for the control current switching the gate into the voltage state is obtained. Note that *LC* resonances, which may be excited in the circuit by the switching process, are suppressed by damping resistors $R_d$.

Another important gate is the Current Injection Device (CID),[36] which is also based on a SQUID as

[35] M. Klein, D.J. Herrel, IEEE J. Solid-State Circuits **13**, 593 (1978).
[36] T. R. Gheewala, IBM J. Res. Dev. **24**, 130 (1980).

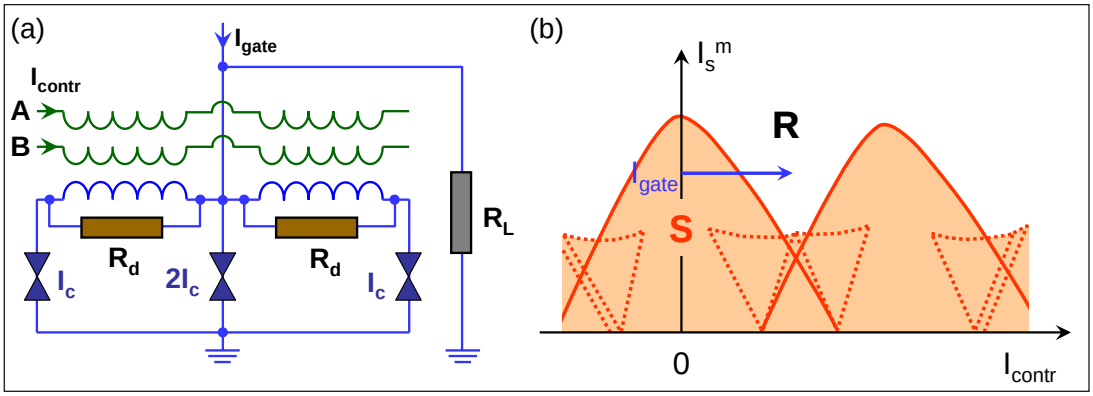


Figure 5.7: (a) Equivalent circuit of a 3-Junction Interferometer Logic (JIL) gate with two inputs A and B. The resistors $R_d$ are damping resistors to damp out $LC$ resonances (the junction capacitances parallel to the ideal Josephson elements are not shown for simplicity). (b) Threshold characteristic $I_s^m(I_{\rm contr})$. The shaded region indicates the superconducting (S) state.

shown in Fig. 5.8. The CID is operated by direct current injection into the SQUID loop. The threshold characteristics can be made symmetric in the two input currents $I_A$ and $I_B$ by a proper choice of the circuit parameters. The CID gate switches to the voltage state with a broad operating window, if both input currents are applied simultaneously. Therefore, the CID can be used as a simple AND gate. However, the CID has no current isolation. A JIL gate in front of a CID gate could be used as current isolation gate.

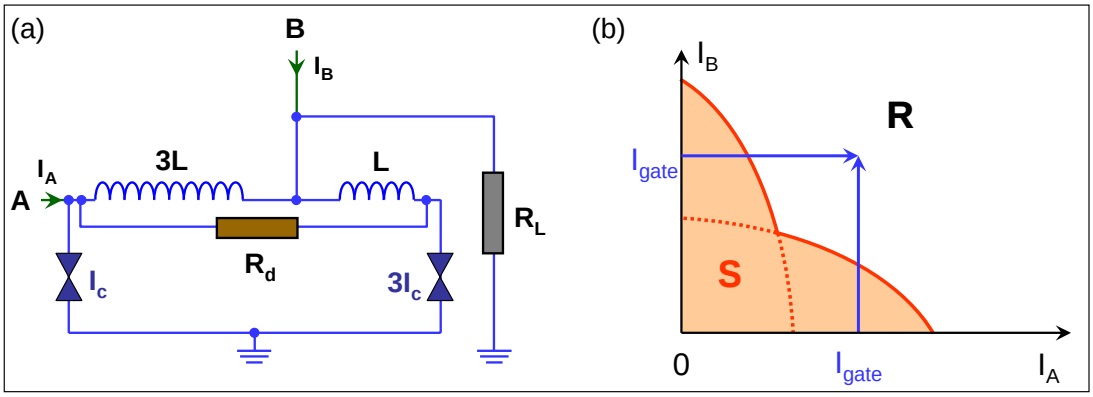


Figure 5.8: (a) Equivalent circuit of the Current-Injection Device (CID). (b) Threshold characteristic $I_A(I_B)$, which is symmetric to the characteristic $I_B(I_A)$. That is, the threshold characteristics is symmetric in the two input currents $I_A$ and $I_B$. No gate current is required.

The operation of JIL and CID gates depends on rather large loop inductances. Therefore, the required areas of these gates are also rather large preventing a high integration density and hence large scale integration of these devices.

### Directly Coupled Gates

Directly coupled gates are controlled by direct injection of the input currents. Note that in the CID described above the magnetic field generated by the injected currents is used to operate the gate. That is why the CID is classified as a magnetically coupled gate. A main advantage of directly coupled devices is the fact that inductances can be eliminated and the devices can be made small.

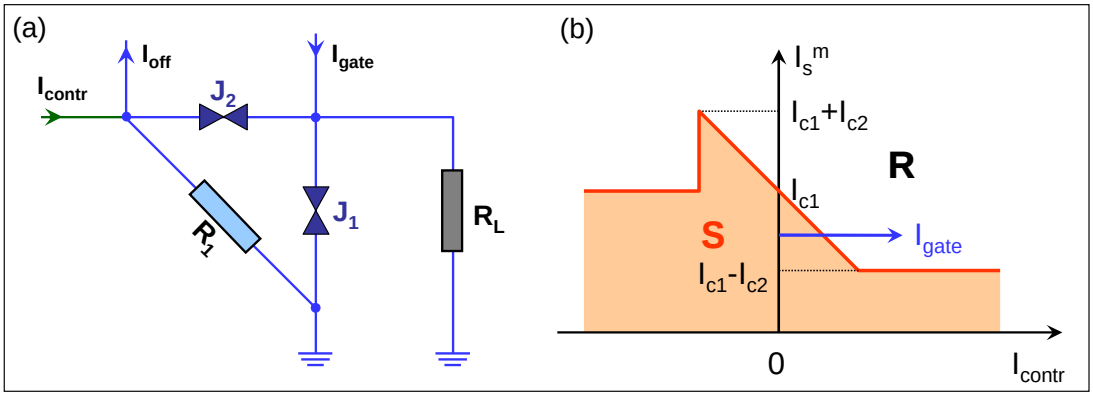


Figure 5.9: (a) Equivalent circuit of the Josephson Atto Weber Switch (JAWS) gate. (b) Threshold characteristic of the JAWS. The input-output current isolation is achieved by the junction $J_2$ and the resistor $R_1$. $I_s^m$ is the maximum current that can be applied via the gate line without switching junction $J_1$ into the voltage state.

An important issue in directly coupled gates is the realization of the current isolation functions. The first device satisfying this requirement is named ***Josephson Atto Weber Switch (JAWS)***.[37] As shown in Fig. 5.9, the JAWS consists of two Josephson junctions and a resistor. The gate is biased with a current $I_{\text{gate}}$ below the critical current $I_{c1}$ of junction $J_1$, i.e. the current flows through $J_1$ and the gate stays in the superconducting state. An input current $I_{\text{contr}}$ through junction $J_2$ increases the current through $J_1$ to $I_{\text{gate}} + I_{\text{contr}}$, which switches $J_1$ to the voltage state. After $J_1$ has switched, $I_{\text{gate}}$ flows through $J_2$ and a small resistor $R_1$ to the ground and $J_2$ also switches to the voltage state. As a result, $I_{\text{gate}}$ is transferred to a load resistor $R_L$ and $I_{\text{contr}}$ flows through $R_1$ to the ground thus providing the current isolation.

Another current isolated gate is the ***Directly Coupled Logic (DCL) gate***[38] shown in Fig. 5.10. The operating principle is similar to that of the JAWS gate. For both the JAWS and DCL gate the threshold curves separating the superconducting from the voltage state have a slope $\Delta I_{\text{gate}}/\Delta I_{\text{contr}} = -1$. For higher slopes ($|\Delta I_{\text{gate}}/\Delta I_{\text{contr}}| > 1$) a higher sensitivity is obtained.

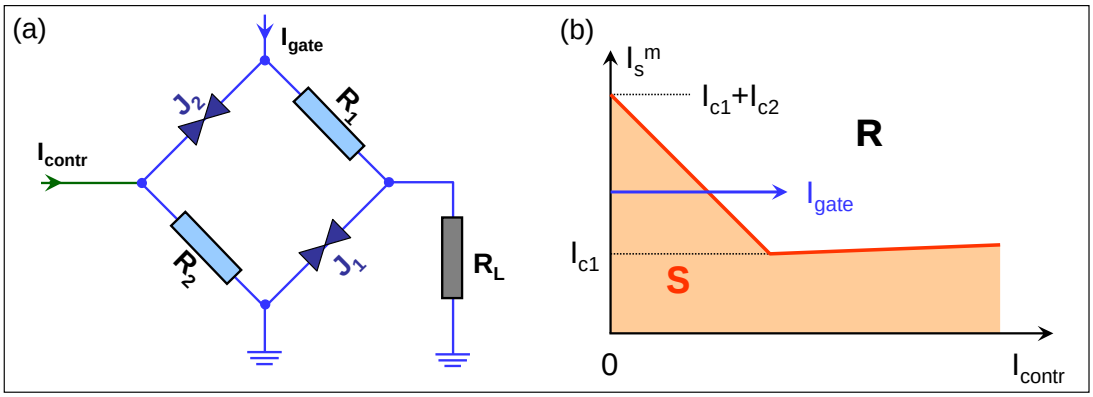


Figure 5.10: (a) Equivalent circuit of the Directly Coupled Logic (DCL) gate. (b) Threshold characteristic of the DCL gate. $I_s^m$ is the maximum current that can be applied via the gate line without switching junction $J_1$ into the voltage state.

The gates shown in Fig. 5.11 have a higher sensitivity or gain compared to the JAWS or DCL gates by inserting an additional Josephson branch. These gates are called ***Resistor Coupled Josephson Logic***

[37] T. A. Fulton, S.S. Pei, L.N. Dunkleberger, Appl. Phys. Lett. **34**, 1876 (1979).

[38] T. R. Gheewala, A. Mukherjee, in *Tech. Digest International Electron Device Meeting (IEDM)*, p. 482 (1979).

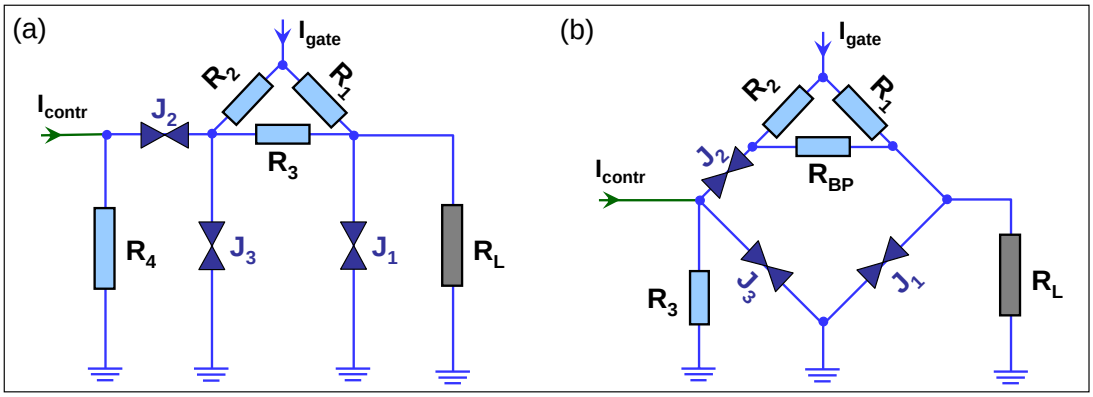


Figure 5.11: Equivalent circuits of (a) the Resistor Coupled Josephson Logic (RCJL) and (b) the Resistor Coupled Logic (RCL) gate. An additional Josephson branch ($J_3$) enhances the sensitivity or gain compared to the JAWS and DCL gates.

***(RCJL)***[39] and ***Resistor Coupled Logic (RCL)***[40]. We note that also modified versions of the RCJL and RCL gates shown in Fig. 5.11 with improved threshold characteristics have been designed.

The ***4 Junction Logic (4JL) gate*** [41] shown in Fig. 5.12 is constructed of 4 Josephson junctions, which are coupled together in a loop. The essential feature of the 4JL gate is that the geometric loop inductance can be made as small as possible and therefore the threshold curve depends entirely on the phase differences across the junctions. The current isolation is realized by introducing a small resistor $R_i$ at the input terminal and by making junction $J_1$ to switch at the final stage of the switching sequence. Based on this 4JL concept an AND gate was realized.

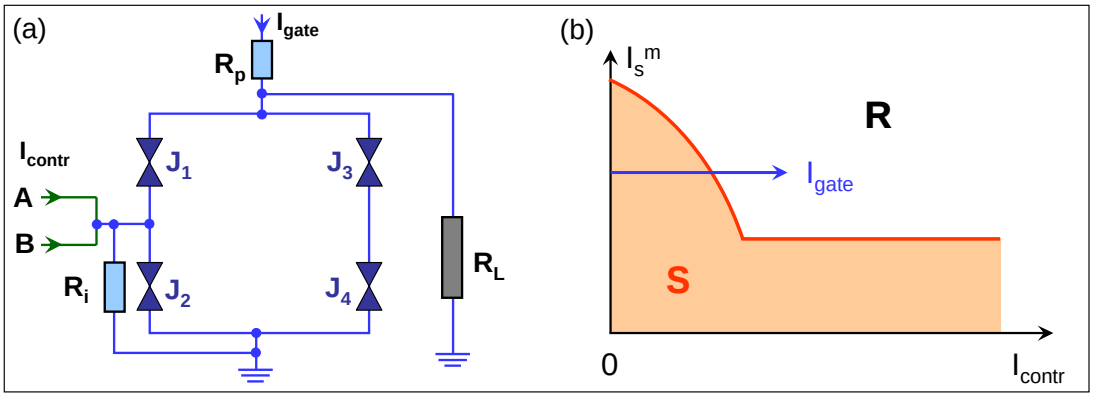


Figure 5.12: (a) Equivalent circuit and (b) threshold characteristic of the 4 Junction Logic (4JL) gate.

The advantage of direct coupled gates over magnetically coupled gates is the elimination of the loop inductance. The 4JL gates for example have been realized with a size of 1200 $\mu$m$^2$, whereas a JIL gate based on the same design rules has an area of 4400 $\mu$m$^2$.

Hybrid devices with both magnetic and direct coupled gates have also been investigated. In the ***Modified Variable Threshold Logic (MVTL)***[42] the input current is first fed into a SQUID control line and then injected into the SQUID directly resulting in a very high sensitivity of the device.

[39] J. Sone, T. Yoshida, H. Abe, Appl. Phys. Lett. **40**, 886 (1982).
[40] K. Hohkewa, M. Okada, A. Ishida, Appl. Phys. Lett. **39**, 653 (1981).
[41] S. Takada, S. Kosada, H. Hayakawa, Jpn. J. Appl. Phys. Suppl. **19-1**, 601 (1981).
[42] N. Fujimaki, S. Kotani, S. Hasuo, T. Yamaoka, Jpn. J. Appl. Phys. **24**, L1 (1985).

### Switching Delay of Logic Gates

In Table 5.1 the logic delays and the power dissipation measured for several gates are listed. The shortest delay of 2.5 ps was obtained for the MVTL fabricated with 1.5 $\mu$m Nb/$AlO_x$/Nb Josephson junctions. However, this should not suggest the superiority of the MVTL, because most of the experiments with the other gate types have been made at an early stage when only the Pb-alloy junction technology was available. Gate delays could be significantly shorter for devices fabricated with modern Nb-technology.

Table 5.1: Switching delay and power dissipation for various types of logic gates.

| gate | linewidth ($\mu$m) | switching time (ps) | power dissipation ($\mu$W) | junction technology | Ref. |
|---|---|---|---|---|---|
| CIL | 2.5 | 13 | 2 | Pb-alloy | [a] |
| JAWS | 5 | 13 | | Pb-alloy | [b] |
| RCJL | 5 | 10.3 | 11.7 | Pb-alloy | [c] |
| RCL | 2 | 4.2 | | Pb-alloy | [d] |
| 4JL | 2.5 | 7 | 4 | Pb-alloy | [e] |
| DCL | 1.5 | 5.6 | 4 | NbN/Pb-In | [f] |
| MVTL | 1.5 | 2.5 | 4 | Nb/$AlO_x$/Nb | [g] |

[a] T.R. Gheewala, A. Mukherjee, in *Tech. Digest International Electron Device Meeting (IEDM)*, p. 482 (1979).
[b] S.S. Pei, Appl. Phys. Lett. **40**, 739 (1982).
[c] J. Sone, T. Yoshida, S. Tahara, H. Abe, Appl. Phys. Lett. **41**, 886 (1982).
[d] J. Nakano, Y. Mimura, K. Nagata, Y. Hasumi, T. Waho, in *Ext. Abstr. of 16th Conf. Solid State Dev. and Mat.*, Kobe (1984), p. 636.
[e] H. Nakagawa, T. Odake, E. Sogawa, S. Takada, H. Hayakawa, Jap. J. Appl. Phys. **22**, L297 (1983).
[f] Y. Hatano, T. Nishino, Y. Tarutani, U. Kawabe, Appl. Phys. Lett. **44**, 1095 (1984).
[g] S. Kotani, T. Imamura, H. Hasuo, in *IEEE IEDM Techn. Digest*, p. 865 (1987).

### Logical Operations

The gates described above can be used for the realization of basic gate operations such as AND, OR and NOT. It is a well known theorem of binary logic that any arbitrary complex logical operation can be expressed in terms of the basic operations AND, OR and NOT. If the control current applied to one of the two control lines A and B is able to reduce the maximum supercurrent $I_s^m$ below the applied gate current, the JIL gate acts as an OR gate. The devices switches to the resistive (R) state, if a control signal is present either at input A or B or at both A and B. Only if no control signal is present at both input channels, the device stays in the superconducting (S) state. If only the sum of the control currents at both input channels is able to reduce $I_s^m$ below the applied gate current, the JIL gate acts as an AND gate. Then, the device stays in the *S* state, if no input signal is present in both or a single input channel. Switching to the R state occurs only, if input signals are present in both channels. The realization of the NOT operation is not as simple. The NOT operation requires that an input with $V \neq 0$ (finite control current) would generate an output $V = 0$ and vice versa. In order to realize this operation the ***dual-rail logic*** can be used, in which both the binary signal and its complement are carried in parallel throughout the entire set of logic operations. Using the dual rail system one can construct a unit cell consisting of two OR and a single AND gate that allows to implement all the required basic gate operations.[43]

[43] H. Hayakawa, *Computing*, in *Superconducting Devices*, Steven T. Ruggiero, David A. Rudman (eds.), Academic Press Inc., San Diego (1990).

### 5.2.5 Memory Cells

Memories are essential components of any computing system. Most digital systems require memory elements that can store and retrieve binary information on the same time scale as the operation of the logic gates. Such memory is acting as the fast cache memory of a computer system. Semiconducting memories rely on electrical charge stored on capacitors with the logical "0" and "1" corresponding to zero and finite charge, respectively. Here, finite charge means typically a few 1000 electrons on a sub-$\mu$m$^2$ capacitor. In superconducting devices it is natural to use persistent currents or magnetic flux stored in superconducting loops for binary information storage.[44] Again, the logical "0" and "1" correspond to zero and finite flux in the loop. Usually, in superconducting circuits only a single flux quantum in the loop is representing the logical "1". In addition to the superconducting loop, READ and WRITE gates are required for fast read out and write in the binary information. Just as for logic circuits, Josephson gates based on hysteretic Josephson junctions can be used to implement a complete memory cell with READ and WRITE gate.[45]

The various memory cells can be divided into ***Non-Destructive Read-Out (NDRO)*** and ***Destructive Read-Out (DRO)*** memory cells. The information stored in non-destructive memory cells can be retrieved without changing the cell state. The NDRO cell is useful to realize cache memories that communicate directly with a central processing unit (CPU). For such application the speed is important, since the memory cell must be capable to store and retrieve binary information at the clock speed of the CPU.

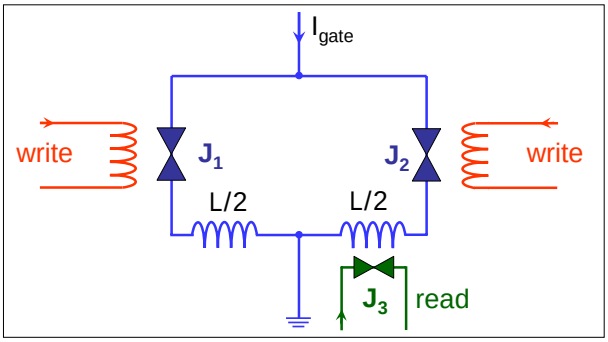


Figure 5.13: Equivalent circuit of the Non-Destructive Readout (NDRO) memory cell.

The earliest NDRO memory cell was suggested in 1969 by **Anacker**[46] and implemented by **Zappe**.[47] Fig. 5.13 shows the operation principle of a NDRO cell. Information is represented as magnetic flux enclosed in the loop (e.g. "0": no flux in the loop, "1": a single or several flux quanta in the loop). In order to discuss the operation principle we start with a loop containing no magnetic flux. If we are biasing the cell by a current $I_{\rm gate}$, due to the symmetry of the cell the current through each of the junctions $J_1$ and $J_2$ is $I_{\rm gate}/2$ for zero writing current. That is, no flux is written into the loop. This corresponds to the "0" state of the loop. If we are now applying a finite writing current to the WRITE gate, we are coupling magnetic flux into the loop. Of course the loop tries to shield this magnetic flux by a circulating current. However, if the write current $I_w$ is large enough, this circulating current exceeds the critical current $I_c$ of the junctions and magnetic flux is entering the loop. If we are now switching off the write current again, the loop keeps the magnetic flux trapped, if the product $LI_c$ of the loop inductance and the critical current of the junctions is larger than $\Phi_0$. Depending on the magnitude of the screening parameter $\beta_L = 2LI_c/\Phi_0$ (compare section 4.1) and the applied write current a single or several flux quanta are trapped in the loop. The state represents the logical "1".

[44] J. Matisoo, *Overview of Josephson Technology Logic and Memory*, IBM J. Res. Develop. **24**, 113 (1980).
[45] Y. Wada, *The Josephson Memory Technology*, Proc. IEEE **77**, 1194 (1989).
[46] W. Anacker, IEEE Trans. Magn. **5**, 968 (1969).
[47] H.H. Zappe, IEEE J. Solid State Circuits **10**, 12 (1975).

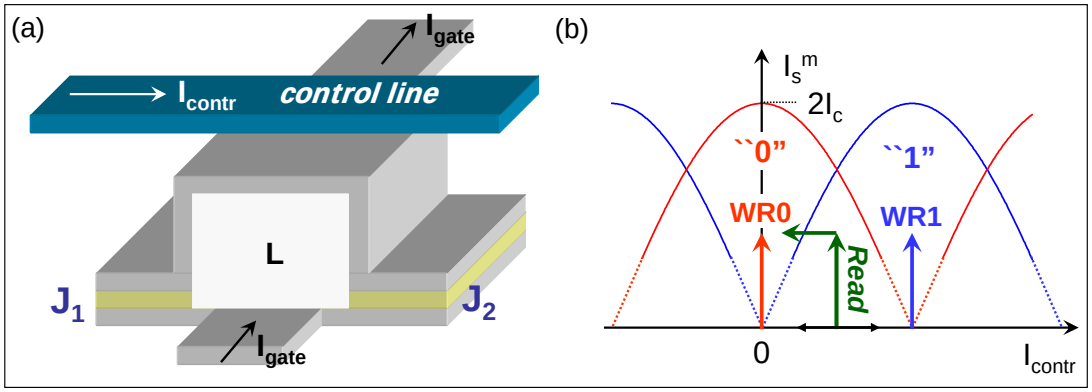


Figure 5.14: (a) Sketch of a Destructive Read-Out (DRO) memory cell and (b) its threshold characteristic. The two-junction SQUID loop has inductance $L = \Phi_0/2I_c$.

The circulating current in the loop can be used as the control current of a READ gate. In Fig. 5.13 the READ gate consists of junction $J_3$. This junction is biased at a current smaller than its critical current. Then, without any circulating current, i.e. no flux in the loop, the junction $J_3$ is in the superconducting or zero-voltage state. However, if there is flux stored in the loop, the corresponding circulating current suppresses the maximum Josephson current of junction $J_3$ to a value below the bias current forcing this junction to switch into the voltage state. The information in the cell can be read out repeatedly without affecting the magnetic flux. That is, the cell acts as a NDRO cell.

An alternative, more compact memory cell is obtained by using only a single two-junction SQUID but in a different operation mode. Fig. 5.14 shows the equivalent circuit and the threshold characteristics of such a Destructive Read-Out (DRO) memory cell[48]. It consists of a symmetrically biased SQUID with two identical junctions with critical currents $I_c$ and loop inductance $L$. The loop inductance is chosen that $2LI_c = \Phi_0$, i.e. $\beta_L = 1$. In this case the two-junction SQUID has a threshold characteristic with overlapping regions of vortex modes where either of the states is stably maintained. For $\Phi = 0$, i.e. no flux in the loop, the threshold characteristic is peaked at $I_{\rm contr} = 0$. For $\Phi = \Phi_0$, i.e. a single flux quantum in the loop, the threshold curve is peaked at a $I_{\rm contr}$ value corresponding to an applied flux of one flux quantum.

In the DRO shown in Fig. 5.14 information is stored in a single flux quantum by using the mode overlapping region. When the operating point moves across the curve there are two different kinds of transitions: the flux transition and the voltage transition. When the operating point crosses the dashed lines in Fig. 5.14 (flux transition) the flux mode is changed without generating a voltage (only a voltage spike is generated). When the operating point moves across the solid lines the cell generates a voltage. To write a "1" the currents $I_{\rm contr}$ and $I_{\rm gate}$ are used to move the operating point across the vortex transition along the arrow WR1 to the $n = 1$ state. To write "0" the operating point must be moved along WR0 to the $n = 0$ state. To read the cell the operating point is moved across the voltage transition line as depicted in Fig. 5.14. Only if the cell had been in the "1" state a voltage is generated. By reading out the cell the information stored in the cell is erased. Therefore, the cell content needs to be refreshed after each read-out process.

We note that the memory cells described above are idealized simple examples. Those memory cells (e.g. the variable threshold memory cells[49]) that have been used in real digital systems are more complex.

[48] H. H. Zappe, Appl. Phys. Lett. **25**, 424 (1974).
[49] I. Kurosawa, A. Yagi, H. Nakagawa, H. Hayakawa, Appl. Phys. Lett. **43**, 1067 (1983).

Table 5.2: Josephson 4 kbit RAM characteristics (organization: 4096 word x 1 bit, NEC).

| | |
|---|---|
| access time | 380 ps |
| power dissipation | 9.5 mW |
| bit yield | 99.8 % |
| Josephson junctions | $Nb/AlO_x/Nb$ |
| number of junctions | 21.000 |
| critical current density | $3.3\,kA/cm^2$ |
| minimum junction size | $2\,\mu m \times 2\,\mu m$ |
| minimum line width | $1.5\,\mu m$ |
| cell size | $55\,\mu m \times 55\,\mu m$ |
| RAM size | $4.5\,mm \times 4.5\,mm$ |

**Performance of Josephson Memory**

The performance of the Josephson memory cells has been improved considerably over the years. Particularly noteworthy are the refinements in Josephson RAM at NEC. The use of moats to control flux trapping and careful attention to the fabrication process has enabled the increase in size to 4 kbit organization and a reduction in critical path access time to below 400 ps. The memory is based on $55 \times 55\,\mu m^2$ vortex transition cells. Table 5.2 summarizes the status of the NEC memory work. This size, however, is still inadequate for most applications. Using a shrink of design rules to submicron features, NEC also has demonstrated an $8.5 \times 11.5\,\mu m^2$ cell which the researchers project to $1\,Mb/cm^2$ density.[50] Nevertheless, much effort remains to solve the memory deficiency of superconductive technology.

### 5.2.6 Microprocessors

Different elements such as logic gates, memory cells, address latches, decoders, power supply schemes, timing control circuits have to be functionally integrated to demonstrate the feasibility of Josephson computer systems. Fig. 5.15 shows the block diagram of an early 4 bit Josephson microprocessor,[51] which is representative of a realistic computer model. The circuit consisting of 64 bit NDRO RAM, ALU, and control circuit was realized through 1841 gates using $2.5\,\mu m$ Nb technology. A typical operation, a carry signal processed in the ALU transferred to the RAM, was performed with a maximum clock frequency of 770 MHz. Table 5.3 summarizes the performance of various logic circuits that have been realized in the 1980s using Josephson latching logic.

Until the end of the 1990s voltage state Josephson logic circuits were continuously improved mainly within the Japanese Josephson Computer Project (participation by the Electrotechnical Laboratory (ETL) and the Central Research Laboratories of Fujitsu, Hitachi, and NEC) . The accomplishments included (i) the reduction to practice and exploitation of the trilayer Josephson junction process, (ii) the demonstration of GHz clock speed for a 8-bit DSP chip with 23 000 junctions and (iii) the fabrication of 380 ps 1 kbit and 4 kbit memories. Particularly noteworthy is the Fujitsu effort that produced 3000-gate (24 000-junction) microprocessor circuits with $1.5\,\mu m$ diameter junctions and demonstrated functionality at a 1.1 GHz clock speed. Other examples are somewhat less complex microprocessors at Hitachi and ETL, as well as random access memory (RAM) of 1-4 kbit at ETL, Fujitsu, and NEC. Fabricated memories were as fast as 380 ps. Late in the project, work was initiated at ETL to combine multiple chips into a high-speed package, and at Fujitsu an innovative through-the-Dewar-wall packaging scheme was demonstrated for

[50] H. Numata, S. Nagasawa, S. Tahara, IEEE Trans. Appl. Supercond. **AS-7**, 2282-2287 (1996).
[51] S. Kotani, IEEE ISSCC Digest of Technical Papers, p. 150 (1988).

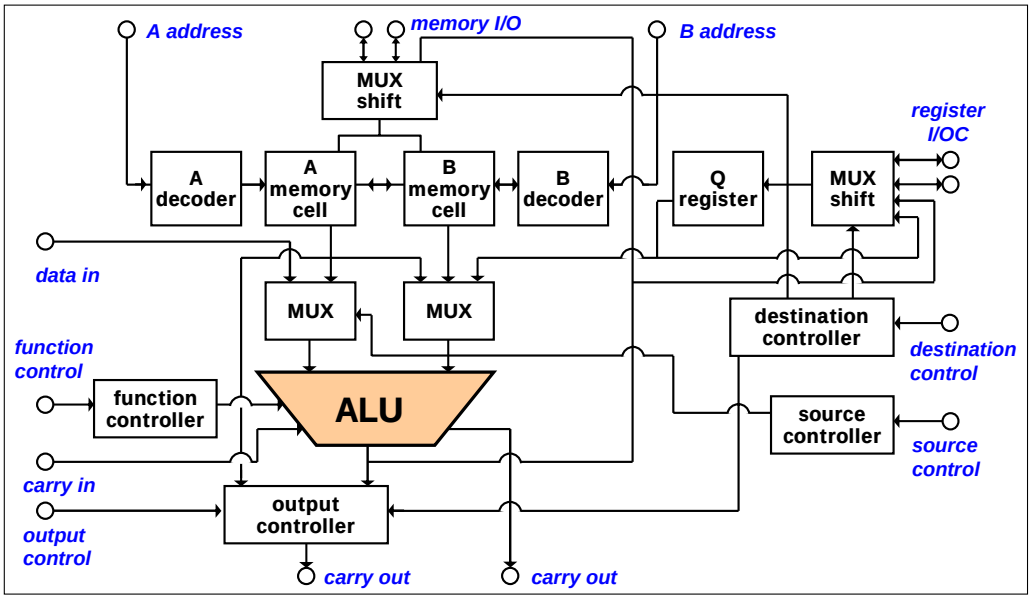


Figure 5.15: Block diagram of the 4 bit Josephson microprocessor (after H. Hayakawa, in *Superconducting Devices*, Steven T. Ruggiero, David A. Rudman (eds.), Academic Press Inc., San Diego (1990).

high-speed operation. After the discovery of the high temperature superconductors in 1986 the activities on low-$T_c$ digital Josephson electronics was reduced considerably also in Japan.

Table 5.3: Performance of various logic gates

| circuit | gate family | junction type | # of gates | performance | Ref. |
|---|---|---|---|---|---|
| 8 bit adder | 4JL | Pb-alloy | 300 | add time 300 ps | [a] |
| 8 bit adder | 4JL | NbN/oxide/NbN | 364 | add time 700 ps | [b] |
| 4 bit adder | RCJL | Pb-alloy | 56 | add time 172 ps | [c] |
| 4 bit multiplier | 4JL | NbN/oxide/NbN | 652 | mult. time 1 ns | [d] |
| 4 bit multiplier | RCJL | Pb-alloy | 249 | mult. time 280 ps | [e] |
| 4 bit multiplier | JTHL | Nb/$AlO_x$/Nb | 104 | mult. time 210 ps | [f] |
| 16 bit multiplier | MVTL | Nb/$AlO_x$/Nb | 828 | mult. time 1.1 ns | [g] |

[a] H. Nakagawa, in *"Extended Abstracts of 15th Conf. on Solid-State Devices and Materials"*, p. 137 (1983).
[b] S. Kosaka, IEEE Trans, Magn. **21**, 102 (1985).
[c] J. Sone, ***in*** "Technical Digest Int. Electron Device Meeting (IEDM)", p. 765 (1982).
[d] S. Kosaka, IEEE Trans, Magn. **21**, 102 (1985).
[e] J. Sone, IEEE Solid-State Circuits **20**, 1056 (1985).
[f] H. Hatano, in *"ISSCC Digest of Tech. Papers"*, p. 196 (1986).
[g] S. Kotani, IEEE J. Solid-State Circuits **22**, 98 (1987).

### 5.2.7 Problems of Josephson Logic Gates

Although the Josephson logic gates and memory cells based on underdamped Josephson junctions can be used to built a Josephson microprocessor, the voltage state Josephson logic suffers several problems that so far prevented their practical use:

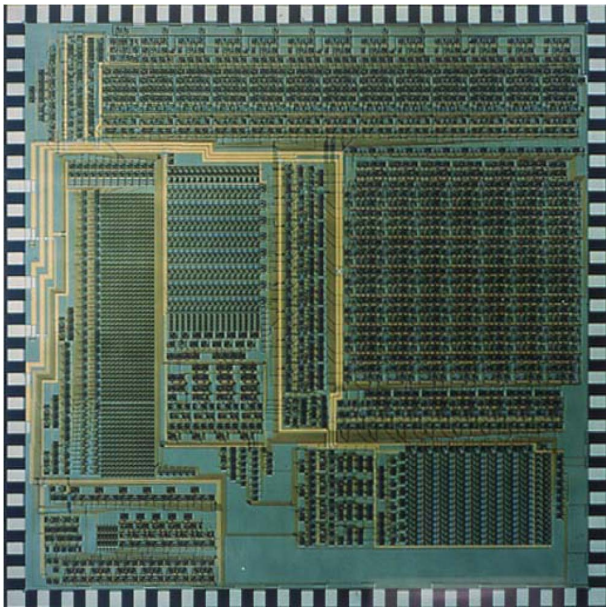

Figure 5.16: Optical micrograph of a Josephson microprocessor.

- The first attempts of IBM to fabricate logic gates were based on unreliable Pb-alloy technology (large parameter spread, unstable against repeated thermal cycles). This problem has been solved by the more appropriate Nb-technology, which provided a significant improvement for the junction quality and reproducibility.
- The voltage state Josephson logic is a latching logic, i.e. switching the junction back to the $V = 0$ state can not be achieved by switching off the control current but requires to switch off the gate current. As discussed above this results in the following complications:
  - an ac power supply is needed,
  - the punchthrough phenomenon limits clock frequencies to $\sim 1$ GHz,
  - a global timing scheme is needed,
  - the junctions switch to the voltage state very fast ("0"$\rightarrow$ "1": 1-10 ps), however, switching back is slow ("1"$\rightarrow$ "0": $\sim 1$ ns).
- There is no transistor-like 3-terminal device providing significant amplification.

## 5.3 RSFQ Logic

To overcome the limitations of the Josephson latching logic based on underdamped Josephson junctions the ***Resistive*** or ***Rapid Single Flux Quantum (RSFQ) logic*** has been proposed.[52,53,54] This nonlatching logic family is based on overdamped Josephson junctions. Since these junctions do no longer have hysteretic IVCs, the information can no longer be encoded in different voltage states of the junctions. In contrast, a totally different representation of information based on single flux quantum (SFQ) pulses is used. The specific properties of the RSFQ logic are:

- nonlatching logic,
- clock frequencies above 100 GHz,
- requirement of overdamped Josephson junctions,
- low power consumption: $P_{\text{diss}}\tau \simeq 10^{-18}$ J per bit.

In order to see the basic difference between the latching and nonlatching Josephson logic we consider Fig. 5.17. In Fig. 5.17a we have sketched the simplest logic gate, the buffer stage, used in latching logic. It employs an underdamped Josephson junction and thus exhibits a hysteretic IVC shown in Fig. 5.17b. The junction is biased at $I_{\text{gate}} < I_c$ so that the junction initially is in its superconducting state ($V = 0$, logical "0"). A control current $I_{\text{contr}}$ drives the total junction current beyond $I_c$ and triggers its switching to its resistive state ($V = 2\Delta/e$, logical "1"), so that a considerable part of the current is steered into the load $R_L$ (typically, through a microstrip line). The latter current serves as an output signal. As we have discussed above, the "0"→ "1" switching process can be very fast (a few ps). However, due to the latching nature of the logic the reset ("1"→"0" switching) cannot be achieved by just turning off $I_{\text{contr}}$ but requires to switch off the bias current $I_{\text{gate}}$. Unfortunately, this operation mode has severe drawbacks as discussed above.

As a result of these drawbacks, no prospects have been found to increase clock frequencies of latching-logic circuits beyond a few GHz. This speed is only comparable to that of semiconductor digital circuits which do not require helium refrigeration. Hence, the only advantage of superconducting voltage state digital circuits would be their smaller power consumption. However, this advantage is not sufficient to warrant commercial introduction of this digital technology. This is why much attention was turned to the alternative ***flux-state*** or ***Single-Flux-Quantum (SFQ)*** logic, which uses coding of the binary information not by the dc voltage, but by single quanta of magnetic flux ($\Phi_0 = h/2e = 2.07 \times 10^{-15}$Vs). SFQ devices are based on overdamped Josephson junctions with non-hysteretic IVCs (see Fig. 5.17c). Here, the states corresponding to the logical "0" and "1" are those without and with the emission of single flux quantum pulses.

SFQ devices can be divided into two groups, defined by the method used to pass the information between logic circuits. First, in ***static SFQ circuits*** the information is passed in the form of dc flux (or supercur-

[52] K. K. Likharev, O.A. Mukhanov, V.K. Semenov, *Resistive single flux quantum logic for the Josephson-junction technology*, in SQUID'85, W. de Gruyter, Berlin (1985), pp. 1103-1108.

[53] K.K. Likharev, V.K. Semenov, *RSFQ logic/memory family: A new Josephson-junction technology for sub-THz-clock-frequency digital systems*, IEEE Trans. Appl. Supercond. **AS-1**, 3-28 (1991).

[54] K.K. Likharev, *Rapid Single Flux Quantum (RSFQ) Logic*, in *Encyclopedia of Materials: Science and Technology*, Elsevier, Amsterdam (2001).

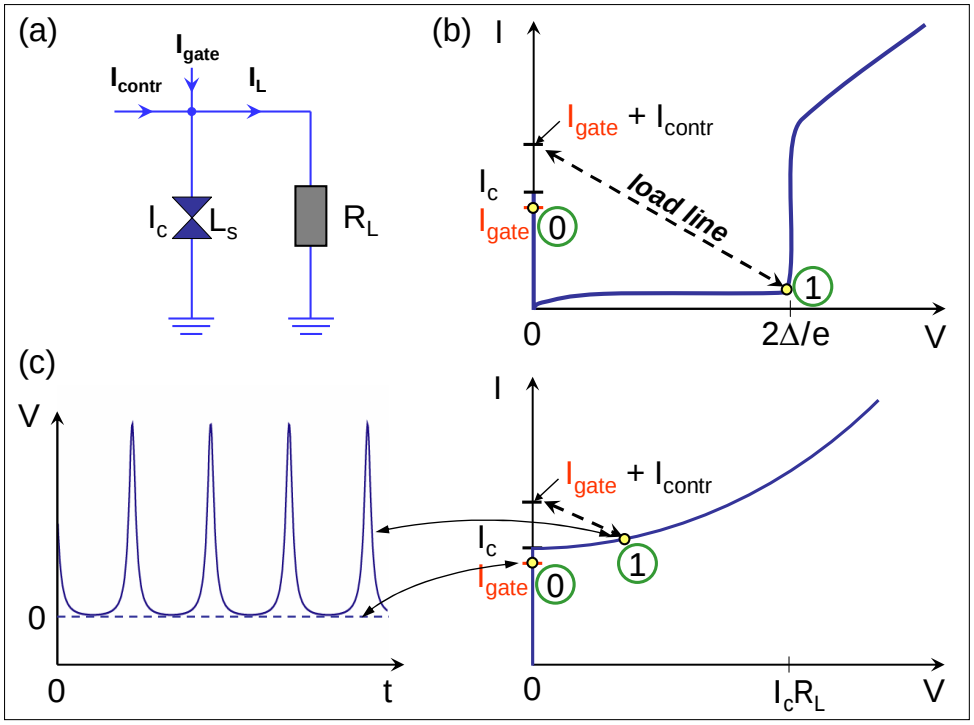


Figure 5.17: (a) Sketch of the buffer stage, the simplest latching logic gate. (b) IVC of an underdamped Josephson junction used for the latching logic. (c) IVC of an overdamped Josephson junction used for the non-latching logic. The states corresponding to the logical "0" and "1" are those without and with the emission of single flux quantum pulses.

rent).[55,56,57,58,59,60] Although these devices are of a high fundamental interest because of their capability to implement the reversible processing of digital information, in static circuits the intergate distance is severely limited (practically, to the nearest neighbors) by the inductance of the interconnects. A further disadvantage of this approach is the need for an rf-supply/clock with similar limitations on speed as for the voltage-state logic. Finally, a detailed analysis shows that parameter tolerances in static SFQ circuits are very low.

In ***dynamic SFQ circuits***[61,62,63,64,65] information between logic devices is passed ballistically, along either passive microstrip lines or active Josephson transmission lines, in the form of very short (picosecond)

[55] C.J. Anderson, M. Klein, M.B. Ketchen, *Transmission of high speed electrical signals in a Josephson package*, IEEE Trans. Magn. **MAG-19**, 1182-1185 (1983).

[56] T.A. Fulton, L.N. Dunkleberger, *Experimental flux shuttle*, Appl. Phys. Lett. **22**, 232-233 (1973).

[57] K.K. Likharev, *Dynamics of some single flux quantum devices. I. Parametric quantron*, IEEE Trans. Magn. **MAG-13**, 242-244 (1976).

[58] J.P. Hurrell, A.H. Silver, *SQUID digital electronics*, in B.S. Deaver Jr. *et al.* (eds.), Future Trends in Superconductive Electronics, AIP, New York (1978), pp. 437-447.

[59] K.K. Likharev, *Classical and quantum limitations on energy consumption in computation*, Int. J. Theor. Phys. **21**, 311-326 (1982).

[60] K.K. Likharev, S.V. Rylov, and V.K. Semenov, *Reversible Conveyor Computation in Array of Parametric Quantrons*, IEEE Trans. Magn. **MAG-21**, 947-950 (1985).

[61] K. Nakajima, Y. Onodera, and Y. Ogawa, *Logic design of Josephson network*, J. Appl. Phys. **47**, 1620-1627 (1976).

[62] K. Nakajima and Y. Onodera, *Logic design of Josephson network - II*, J. Appl. Phys. **49**, 2958-2963 (1978).

[63] C.A. Hamilton, F.L. Lloyd, *100 GHz binary counter based on dc SQUIDs*, IEEE Electron. Dev. Lett. **3**, 335-338 (1982).

[64] A.H. Silver, R.P. Phillips, R.D. Sandell, *High speed nonlatching SQUID binary ripple counter*, IEEE Trans. Magn. **MAG-21**, 204-207 (1985).

[65] K. Nakajima, G. Oya, Y. Sawada, *Fluxoid motion in phase mode Josephson switching system*, IEEE Trans. Magn. **MAG-19**, 1201-1204 (1983).

quantized voltage pulses $V(t)$ associated with a $2\pi$-change of the phase difference across a Josephson junction. According to the Josephson relation $V = \frac{\hbar}{2e}\dot{\varphi}$ it is obvious that the $2\pi$-change results in a voltage pulse of fixed area

$$\int V\,dt \;=\; \int \frac{\hbar}{2e}\,d\varphi \;=\; \frac{h}{2e} \;=\; \Phi_0 \;=\; 2.07\times 10^{-15}\ \mathrm{Vs} \tag{5.3.1}$$

The essence of this idea is that these SFQ pulses can be quite naturally generated, reproduced, amplified, memorized, and processed by elementary circuits comprised of overdamped Josephson junctions. This unique ability, fully realized quite early in some analog devices based on the Josephson effect, was virtually neglected in latching logic. Moreover, in the latching logic circuits the SFQ pulse generation is an inherent reason for the punchthrough effect, which limits operation speed.

Until the mid-1980s, several suggestions on how to use SFQ pulses for processing of digital information and analog-to-digital (A/D) conversion were put forward.[66,67,68,69,70] However, it was only in 1985-86 that a complete family of dynamic SFQ circuits, with the nickname ***Rapid Single-Flux-Quantum (RSFQ)*** was suggested by the group around **K.K. Likharev** at the Moscow State University.[71,72] Until the early 1990s a few circuits containing several of the simplest basic components of the RSFQ family have been fabricated and tested . These components were demonstrated to work at clock frequencies in excess of 100 GHz.[73,74] Simultaneously, numerical simulations had shown that the speed could be increased beyond 300 GHz going from a 5 to a 1 $\mu$m technology. Since the early 1990s the RSFQ idea has been adopted by several groups worldwide.

We also would like to mention that an alternate family of dynamic SFQ devices was suggested under the name ***Phase Mode Josephson System*** by **K. Nakajima** and coworker at Tohoku University, Japan.[75,76]

### 5.3.1 Basic Components of RSFQ Circuits

#### Generation of SFQ Pulses

SFQ pulses are most simply generated by biasing an overdamped Josephson junction slightly above its critical current $I_c$. As we have discussed in section 3.3, the Josephson current $I_s$ in this case flows in form of short pulses across the junction with the pulse duration being of the order of $\Phi_0/2I_cR$ (see Fig. 5.18).

[66] T.D. Clark, J.P. Baldwin *Superconducting memory device using Josephson junctions*, Electron. Lett. **3**, 178-179 (1967).

[67] W. Anacker, H.H. Zappe, *Superconducting memory array using weak links*, U.S. Patent No.: 3705393, filed June 30, 1970; published Dec. 5, 1972.

[68] W.J. Lum, H.W.K. Chan, T. Van Duzer, *Memory and logic circuits using semiconductor-barrier Josephson junctions*, IEEE Trans. Magn. **MAG-13**, 48- 51 (1977).

[69] H.H. Zappe, *A single flux quantum Josephson junction memory cell*, Appl. Phys. Lett. **25**, 424-426 (1974).

[70] H.H. Zappe, *A subnanosecond Josephson tunneling memory cell with nondestructive readout*, IEEE J. on Solid State Circuits **10**, 12-19 (1975).

[71] K. K. Likharev, O.A. Mukhanov, V.K. Semenov, *Resistive single flux quantum logic for the Josephson-junction technology*, in SQUID'85, W. de Gruyter, Berlin (1985), pp. 1103-1108.

[72] O.A. Mukhanov, V.K. Semenov, K.K. Likharev, *Ultimate performance of RSFQ logic circuits*, IEEE Trans. Magn. **MAG-23**, 759-762 (1987).

[73] V.K. Kaplunenko, M.I. Khabipov, V.P. Koshelets, K.K. Likharev, O.A. Mukhanov, V.K. Semenov, I.L. Serpuchenko, A.N. Vystavkin, *Experimental study of the RSFQ logic elements*, IEEE Trans. Magn. **MAG-25**, 861-864 (1989).

[74] L.V. Fillipenko, V.K. Kaplunenko, M.I. Khabipov, V.P. Koshelets, K.K. Likharev, O.A. Mukhanov, V.K. Semenov, I.L. Serpuchenko, A.N. Vystavkin, *Experimental implementation of analog-to-digital converter based on the reversible ripple counter*, IEEE Trans. Magn. **MAG-27**, 2464-2467 (1991).

[75] K. Nakajima, H. Mizusawa, H. Sugahara, Y. Sawada, *Phase mode Josephson computer system*, IEEE Trans. Appl. Supercond. **AS-1**, 29-36 (1991).

[76] K. Nakajima, *Single Flux Quantum Electronics*, in *Handbook of Applied Superconductivity*, Vol. **2**, B. Seeber ed., IOP Publishing, Bristol (1998), pp. 1795-1812.

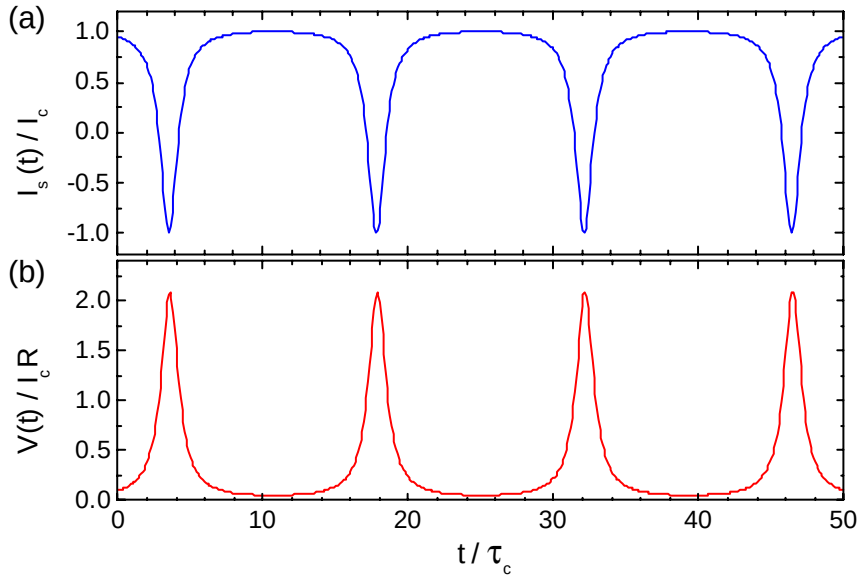


Figure 5.18: Time variation of (a) the Josephson current $I_s$ and (b) the junction voltage $V$ for an overdamped Josephson junctions biased at $I/I_c = 1.05$. The time is normalized to $\tau_c = \Phi_0/2\pi I_c R$.

Here, $1/R = 1/R_N + 1/R_L$ is the total resistance in parallel to the ideal Josephson element. In the best case, $R \sim R_N$ and the pulse duration is given by $\Phi_0/2I_cR_N$, which is about 1 ps for $I_cR_N \sim \Delta/e \sim 1$ mV. Note that superconducting tunnel junctions are usually intrinsically underdamped and have to be brought to the overdamped regime by a small shunt resistance. Than, $I_cR < I_cR_N$ resulting in a longer pulse duration and smaller pulse height. We see that the typical SFQ pulse is smaller in voltage and shorter in time than the typical pulses obtained in voltage state logic.

In order to generate individual SFQ pulses the circuit shown in Fig. 5.17a can be used. A single quantized SFQ pulse may be generated by feeding the Josephson junction by a short non-quantized current pulse $I_{\rm contr}$ arriving from e.g. a semiconductor electronic device. A disadvantage of this circuit is that the pulse should be very short (a few picoseconds), and its duration should be within certain limits.

A less demanding way to generate SFQ pulses is to use a Josephson junction in parallel with the superconducting inductor $L$, that is an rf-SQUID with a screening parameter $\beta_{L,\rm rf} = 2\pi I_c L/\Phi_0$ ranging somewhere between 3 and 10 (compare section 4.2). A slightly modified version is shown in Fig. 5.19a. In order to generate a single SFQ pulse, the interferometer may be fed by a usual dc current pulse, with amplitude (but not length) within certain limits. For example, a periodic train of SFQ pulses can be generated by using an external microwave signal for $I_{\rm contr}$, which can be sent from room temperature via coaxial lines at least up to several 10 GHz. A single SFQ pulse is generated every rf-cycle when the rf-current exceeds the current value $I_1$. The generated pulse train can be distributed to the various gates of a circuit via transmission lines acting as a clock for the circuit. Of course a train of SFQ pulses can be generated also by biasing an overdamped Josephson junction slightly above the critical current as shown in Fig. 5.18b.

Fig. 5.19d shows a more advanced version of such a ***dc to SFQ converter***. If its input current $I_{\rm gate}$ is increased beyond a certain threshold value $I_{\rm high}$, the critical state of the junction $J_3$ is achieved, and the SFQ pulse is generated across it. Simultaneously, the three-junction interferometer ($J_1$-$J_3$, $L_1$-$L_3$) is switched into another flux state. In order to reset the interferometer into its initial state, the current should then be decreased below a value $I_{\rm low}$ at which sequential $2\pi$-jumps are triggered in the junctions $J_1$ and $J_2$. The reset is accompanied by the generation of SFQ pulses across these junctions.

We note that also the inverse of a dc to SFQ converter, a SFQ to dc converter can be implemented.

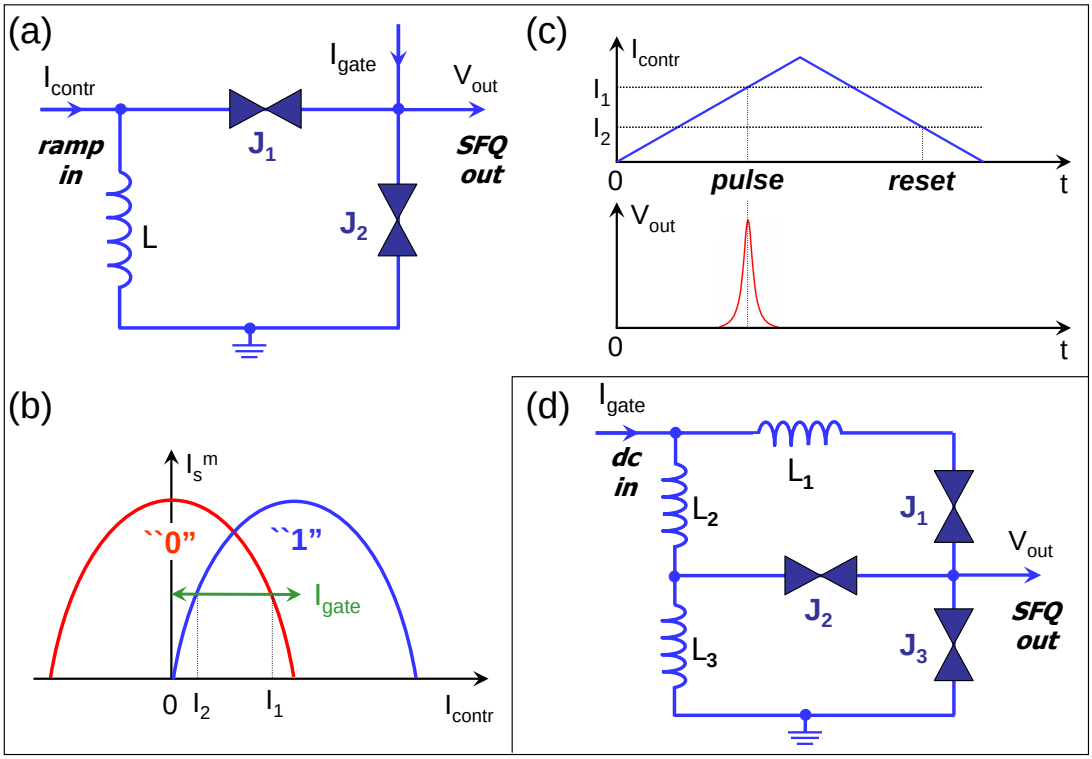


Figure 5.19: (a) Circuit and (b) approximate threshold characteristic of a SFQ pulse generator. $I_1$ and $I_2$ mark the current values for the "0"→ "1" and the return transition, respectively. (c) shows the current ramp used for $I_{\rm contr}$ and the resulting SFQ output pulse. In (d) another possible structure of a dc to SFQ converter is shown that requires only a dc input signal.

### Reproduction, Amplification and Transfer of SFQ Pulses

We have seen that if the dc bias current $I_{\rm gate}$ is not too far from the critical value $I_c$, a SFQ pulse can be triggered by an incoming short control pulse, with either the nominal or a somewhat different amplitude. This means that the simple circuit shown in Fig. 5.19a can reproduce SFQ pulses, bringing their area $\int V(t)dt$ to the nominal value $\Phi_0$, i.e. providing a moderate voltage gain if necessary. On the other hand, if the input pulse is too weak (e.g. a weak noise signal due to parasitic crosstalk between the signal transfer lines) it is not reproduced by the circuit, so that the circuit also serves as a noise discriminator.

**Josephson Transmission Line:** Key elements of RSFQ circuits are Josephson transmission lines (JTL, see Fig. 5.20a) comprising several Josephson junctions connected in parallel by superconducting strips of a relatively low inductance $L \sim \Phi_0/I_c$, and dc-current biased to their sub-critical state ($I_{\rm gate} < I_c$). If the inductance would be much smaller, then a fluxon in the JTL would be spread out over several junctions. On the other hand, if $L$ would be much larger, then several flux quanta could be in a single loop. Upon triggering a $2\pi$-jump of the Josephson phase in the left junction $J_1$ by the input signal A, the resulting SFQ pulse developed across $J_1$ will trigger a $2\pi$-jump in $J_2$, and so on. This is equivalent to a flux quantum moving from left to right. That is, the SFQ pulse is transferred along the Josephson transmission line. It has been shown that 5 ps SFQ pulses can be transferred over distances up to 1 cm without noticeable attenuation. JTLs can also be used to amplify SFQ pulses (or, more exactly, to provide their current/power gain while conserving their voltage area). For that, the critical currents of the junctions and the corresponding dc bias currents should grow in the direction of the pulse propagation, with the proportional decrease of the inductances.

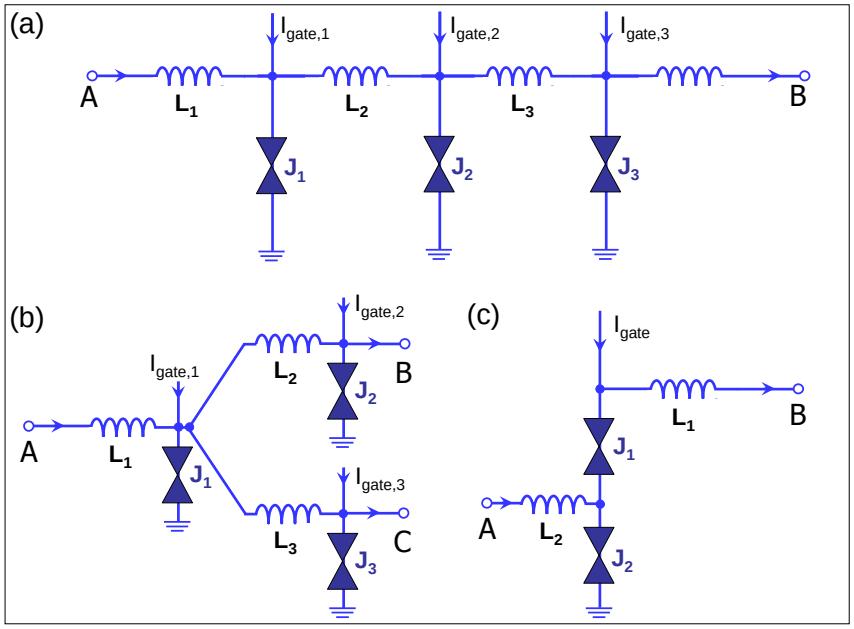


Figure 5.20: Some basic elements of RSFQ circuits: (a) Discrete Josephson transmission line for active SFQ pulse transfer, (b) SFQ pulse splitter, and (c) buffer stage.

Alternatively, a purely passive superconducting transmission line can be used for transmitting SFQ pulses with low loss or dispersion. The impedance of this line should be close to that of the shunt resistor $R_L$ for good matching. However, the nonlinear active transmission line shown in Fig. 5.20a has the advantage that it automatically filters out low-level noise and also regenerates the SFQ pulse.

**SFQ Pulse Splitter:** As shown in Fig. 5.20b, an evident generalization of the JTL can be used to provide splitting of the SFQ pulse, i.e., reproduction of the input pulse A at each of its two outputs B and C, without noticeable decrease of the pulse voltage amplitude. That is, the JTL can be split into two or more lines so that one SFQ pulse can give rise to many such pulses. Note that the pulse splitter is symmetric among its three ports and an SFQ pulse incident from any of these ports will yield an SFQ pulse out along the two others. Again, a splitter also can be achieved by splitting a passive transmission line. However, in this case one has more stringent requirements for the matching condition at the intersection to avoid reflections.

**Buffer Stage:** Unfortunately transmission lines and splitters transmit pulses equally well in both directions and cannot be used for isolation. That is, we need a buffer stage as shown in Fig. 5.20c. The junctions are dc-current biased below their critical currents. If a short pulse arrives at A, it induces a $2\pi$ switching of the Josephson phase of junction $J_2$. This switching produces the standard SFQ pulse at the output terminal B. The input pulse may be weaker than the standard pulse, so that the circuit provides some amplification. On the other hand, if the pulse arrives at terminal B, junction $J_1$ generates a $2\pi$ pulse because of its lower critical current. Thus, no SFQ pulse passes to the input A of the circuit, i.e. it performs the function of a one-directional buffer.

### SFQ Memory Cell

Fig. 5.21 shows the SFQ memory cell also known as the RS flip-flop and DRO register. This standard RSFQ latch essentially consists of a two-junction ($J_1$ and $J_2$) superconducting quantum interferometer

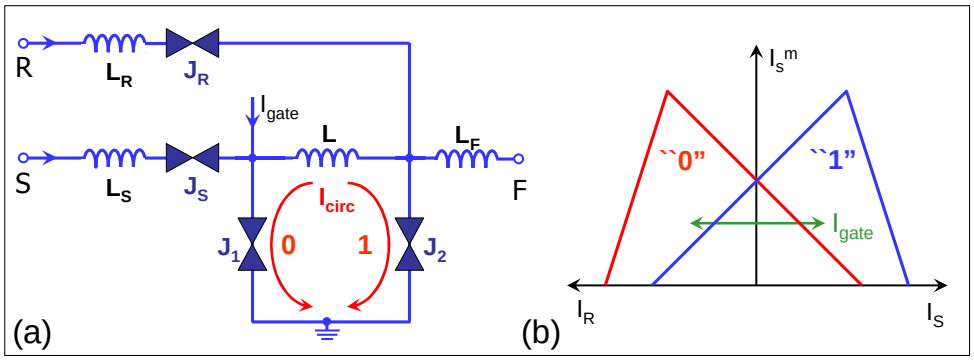


Figure 5.21: (a) Circuit diagram of the SFQ memory cell also known as RS flip-flop. (b) Approximate critical current threshold characteristic for the RS flip-flop showing the zero voltage regime for the "0" and the "1" state as a function of the control currents at the S and the R inputs.

(dc-SQUID) with two input lines each with a buffering series junction ($J_S$ and $J_R$). It stores information in form of quantized flux trapped in the superconducting loop. If the inductance $L$ of the interferometer is chosen so that the screening parameter $\beta_L = 2I_cL/\Phi_0 \sim 3$ and the dc bias current $I_{\rm gate} \sim 0.8\,I_c$, the circuit has two symmetric stable stationary states, which differ with respect to the direction of the persistent current $I_{\rm circ} = \Phi_0/2L$ circulating in the loop. In other words, one of these states corresponds to an additional single flux quantum trapped in the superconducting loop of the interferometer.

Let us suppose that the SQUID is initially in the "0" state with zero flux in the loop. If the bias current $I_{\rm gate}$ is switched on to a value below the critical current of the SQUID, most of the current will flow through the left junction $J_1$ due to the large inductance $L$. Actually, this corresponds to a counterclockwise circulating current with $I_1 = I_{\rm gate}/2 + I_{\rm circ} < I_c$ and $I_2 = I_{\rm gate}/2 - I_{\rm circ}$. If now a SFQ pulse arrives at the input S, it triggers a $2\pi$-jump in junction $J_1$, which is biased close to $I_c$, but not in $J_2$, which carries a lower dc current $I_2 = I_{\rm gate}/2 - I_{\rm circ}$. This corresponds to a fluxon crossing $J_1$ and entering the loop. As a result, the cell is switched to its opposite state 1 with the clockwise circulation of the persistent current $I_{\rm circ}$. It is evident that now the reset (the "1" $\rightarrow$ "0" switching) can be triggered by the SFQ pulse arriving at the R terminal. Simultaneously, an SFQ pulse $V(t)$ is developed across $J_2$, which can serve as an output signal F. This corresponds to a flux quantum leaving the loop through junction $J_2$. The auxiliary junctions $J_S$ and $J_R$ defend the SFQ pulse sources from the back reaction of the interferometer in the case of a "wrong" signal, for example, the S (set) pulse arriving during the state 1. In this case, junction $J_S$ (rather than $J_1$) switches. That is, the incoming single flux quantum drops out of the circuit through $J_S$, if the interferometer loop is unable to accept it. In the same way, if the circuit is in the 0 state, then a readout pulse into the R input will not trigger $J_2$, since the effective bias current is quite small, but rather the right buffer junction $J_R$. Therefore, no output signal will be generated. One can see that for SFQ pulses the circuit works exactly as a standard RS flip-flop (latch): SFQ pulses can be trapped by this circuit, so that the information about their arrival can be conveniently stored there in the form of static magnetic flux, and released when necessary in SFQ pulse form.

At present the absence of large Josephson junction memories is a major problem for the successful application of RSFQ circuits (compare also section 5.2.5). Demonstrated RAM chips had shown a decent access time of the order of a few 100 ps, but only of a few 10 kbit size. However, there is no inherent problem with the implementation of high-density Josephson junction RAMs. But of course their development would require a large investment of effort and money. Right now these resources are not in sight.

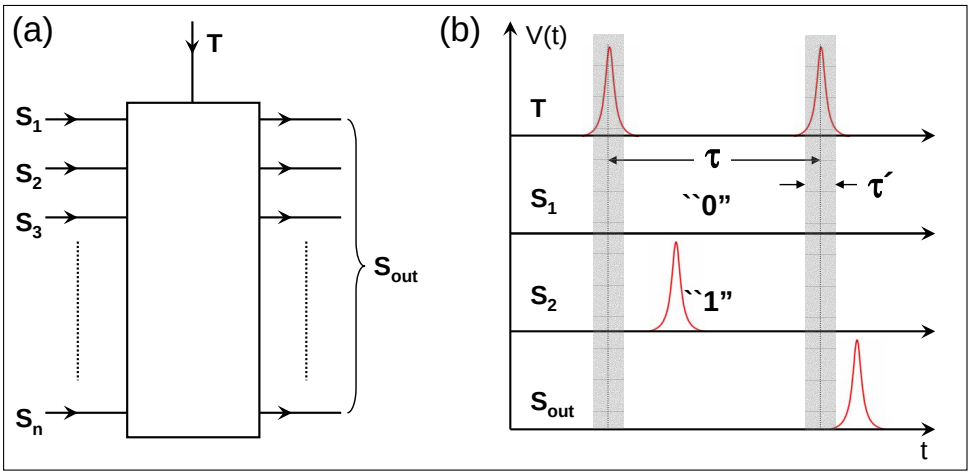


Figure 5.22: Representation of binary units in the RSFQ logic circuits. The signal pulses S are allowed to arrive during the whole clock period $\tau$ except some close vicinity $\tau'$ of the clock pulses (after Likharev *et al.*, IEEE Trans. Appl. Supercond. **AS-1**, 3-28 (1991)).

### 5.3.2 Information in RSFQ Circuits

In order to perform digital operations with signals as unusual as picosecond SFQ pulses, an explicit definition of what digital information is in RSFQ circuits is required. Such a definition was probably the most important conceptual step made by **Likharev** and coworkers.[77]

According to this concept, any RSFQ circuit may be considered as consisting of ***elementary cells*** or ***timed gates*** operating as shown in Fig. 5.22. Each cell has two or more stable flux states. The cell is fed by SFQ pulses, which can arrive from signal lines $S_1, S_2, \ldots, S_n$ and a clock or timing line T. Each clock pulse marks a boundary between two adjacent clock periods by setting the cell into its initial state "1". During the new period, an SFQ pulse can arrive (or not arrive) at each of the cell inputs $S_i$ (see Fig. 5.22b). Then information can be transferred generally through two lines, one carrying short (quasi)periodic clock pulses T, while the other carries the bit pulses $S_i$. The logical value "1" of the signal $S_i$ is characterized by the arrival of a single pulse at terminal $S_i$ between two consecutive T pulses, whereas the absence of a pulse denotes a "0". In Josephson junction circuits this representation is very natural, if single flux quantum (SFQ) pulses of the form $\int V dt = \Phi_0$ are used in both the S and T line. As shown above, such pulses can be readily generated and reproduced/amplified either by single overdamped Josephson junctions or by simple circuits consisting of such junctions.

The convention for representing information in RSFQ circuits does not require the exact coincidence of SFQ pulses in time, nor is a specified time sequence of the various input signals needed. Each pulse can either change or not change the internal state of the cell, but it can not produce any immediate reaction at its output terminal(s) $S_{out}$. Only the clock pulse T is able to fire out the pulse(s) $S_{out}$ corresponding to the internal state of the cell, predetermined by the input signal pulses which have arrived during this period. The same clock pulse terminates the clock period by resetting the cell into its initial state. Thus, an elementary cell of the RSFQ family is equivalent to a usual asynchronous logic circuit coupled with a latch (flip-flop) storing its output bit(s) until the end of the clock period.

[77] K. K. Likharev, O.A. Mukhanov, V.K. Semenov, *Resistive single flux quantum logic for the Josephson-junction technology*, in SQUID'85, W. de Gruyter, Berlin (1985), pp. 1103-1108.

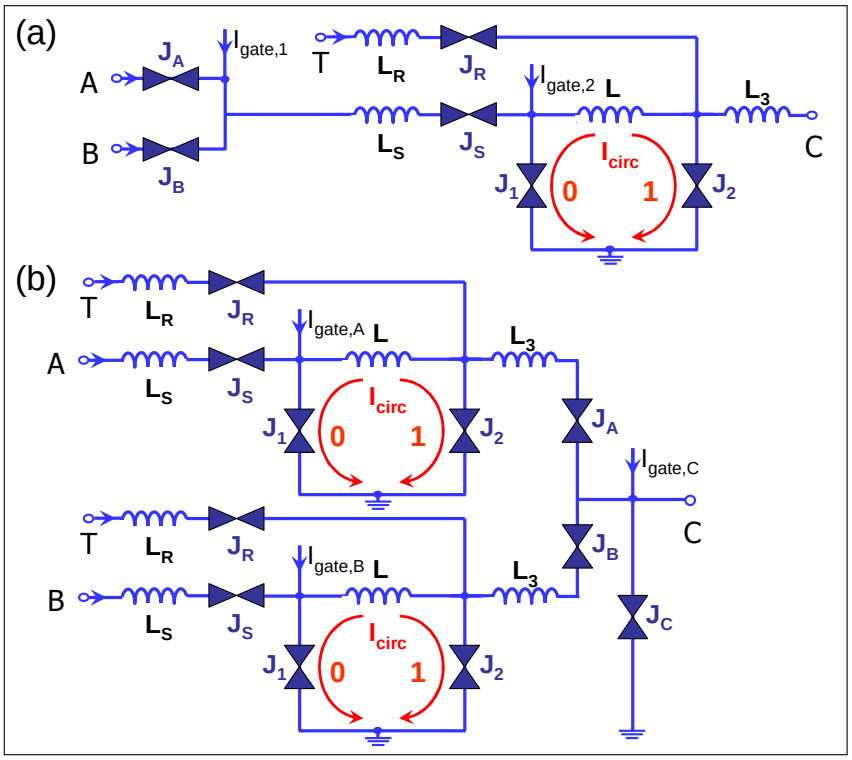


Figure 5.23: Circuit diagram of (a) the triggered OR gate and (b) the triggered AND gate.

### 5.3.3 Basic Logic Gates

**YES Gate:** In addition to being a basic RSFQ memory cell, the RS flip-flop can also function as a latch for a logic state. The data enter the cell from the left and leave it again when a trigger signal enters at the right. We consider the RS flip-flop shown in Fig. 5.21a. We suppose that the input S is fed from a signal line, while the clock pulses are fed into input R. The clock cycle starts from the clock pulse, resetting the system back into its state "0". If no signal pulse S arrived during the current clock cycle, then the new clock pulse R would trigger the SFQ pulse across $J_R$ rather than $J_2$. That is, no output signal appears at F. However, if this concluding clock pulse was preceded by the signal pulse S (switching the interferometer to state "1"), then the clock pulse would trigger the SFQ pulse across $J_2$, which will serve as the output signal. Simultaneously, the flip-flop is reset into state "0". We see that the RS flip-flop in this case works in accordance with the above definition of an RSFQ elementary cell, performing the function YES, i.e. reproducing the input signal S, with its time delay until arrival of the clock pulse. In other words, this circuit works as a 1-bit stage of a shift register. Such RSFQ registers have been tested successfully at frequencies up to 60 GHz with parameter margins up to $\pm 30\%$.[78]

**OR Gate:** We next consider a simple triggered OR gate shown in Fig. 5.23a. It consists of a so-called confluence buffer with its output connected to the input S of an RS flip-flop. For the confluence buffer the bias current of junction $J_1$ partly act as bias for the buffer junctions $J_A$ and $J_B$. A voltage pulse coming in will generate a current that subtracts from the bias current and therefore will not switch the buffer junctions. In contrast, a pulse going out will add to this bias and switch the junction. If two SFQ pulses enter at A and B at different times, only the first fluxon will be stored in the SQUID loop. The second pulse will leave the line across the buffer junction $J_S$. When the timing pulse T is sent, only a single SFQ pulse is generated at the output. It is evident that this circuit functions as an OR gate. Note that four

[78] O.A. Mukhanov, *Rapid single flux quantum (RSFQ) shift register family*, IEEE Trans. Appl. Supercond. **AS-3**, (1993).

out of the six junctions are buffer junctions and only two form the latch. Of course more complicated OR gates with optimized performance, allowing for large parameter spread of the junctions, have been fabricated.[79,80]

**AND Gate:** Fig. 5.23b shows a triggered AND gate, which has an RS flip-flop before each input of a confluence buffer. If the input pulses A and B come in at different times, the input latches serve to store them until they are released simultaneously by the trigger pulse T. This in turn triggers the nearby junction $J_C$, which provides an output pulse only when both inputs were "1". Note that for the AND gate as well as for the OR gate there a several closed superconducting loops, which would be more evident if all the ground lines would be connected. This makes RSFQ circuits sensitive for trapped magnetic flux. That is, sufficient magnetic shielding and the use of moats keeping trapped flux away from the circuits are required.

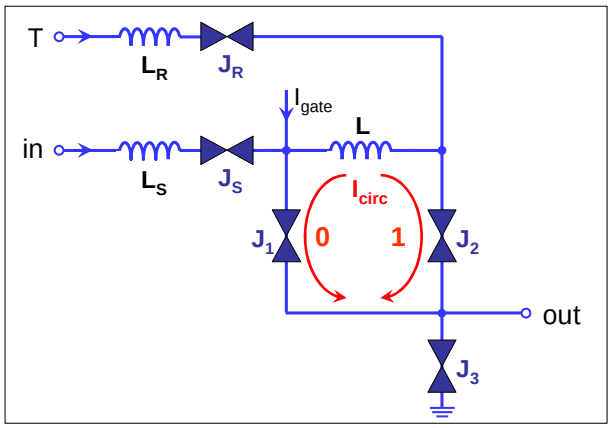


Figure 5.24: Circuit diagram of the RSFQ NOT gate.

**NOT Gate:** Fig. 5.24 shows a possible implementation of an RSFQ inverter. This circuit is also built around a single interferometer ($J_1$, L, $J_2$), but also includes an additional Josephson junction $J_3$. In the initial state "0" the higher current is flowing through $J_1$, while $J_2$ carries virtually no current. This means that in the absence of an input pulse $S_1$, the next clock pulse would trigger the SFQ pulse in $J_3$ rather than in $J_2$, and this pulse would appear at the circuit output $J_3$. That is, an input "0" provides an output "1". If in contrast a signal pulse $S_1$ arrives, it would switch the interferometer into the state "1", with a higher current in $J_2$. In this case, the next clock pulse would trigger the SFQ pulse across $J_2$ rather than $J_3$. That is, the circuit would be reset, and no output pulse developed. In total, an input "1" yields an output "0".

**Shift Register:** We can arrange a large number of RS flip-flops as shown in Fig. 5.25 to obtain a shift register. Here, the bottom row of linked SQUIDs ($\beta_L \sim 3$) represents a series of binary bits. Each cell contains either no (logical state "0") or a single flux quantum (logical state "1"). The upper row of SQUIDs do not store fluxons but rather form a Josephson transmission line that transmits the trigger/reset pulses entering from the right. The shift register operates as a first-in, first-out (FIFO) memory. If the trigger pulse enters, it shifts the contents of the cells a single cell to the right. Then, a new data bit can be inserted at the input on the left.

[79] S.V. Polonsky, V.K. Semenov, P.I. Bunyk, A.F. Kirichenko, A. Yu. Kidiyarova- Shevchenko, O.A. Mukhanov, P.N. Shevchenko, D.F. Schneider, D.Yu. Zinoviev, K.K. Likharev, *New RSFQ circuits*, IEEE Trans. Appl. Supercond. **AS-3** 2566-2577 (1993).

[80] Y.K. Kwong, V. Nandakumar, *Experimental evaluation of some rapid single flux quantum cells*, IEEE Trans. Appl. Supercond. **AS-3**, (1993).

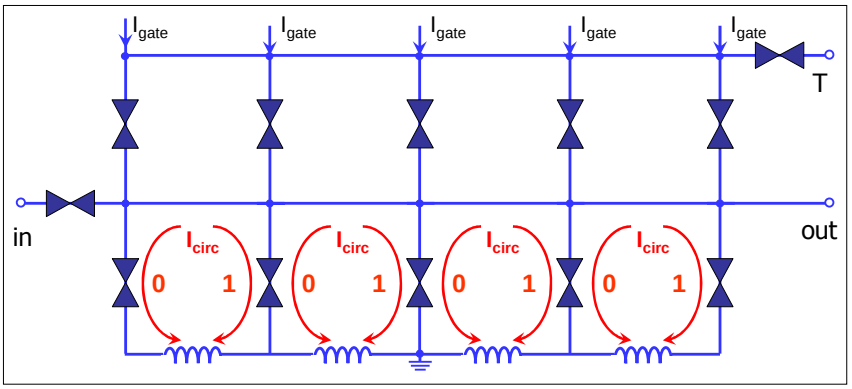


Figure 5.25: RSFQ shift register formed by a series array of RS flip-flops.

### 5.3.4 Timing and Power Supply

At the very high speed of RSFQ circuits timing becomes an issue of primary importance. It is obvious that the use of a global clock is problematic. In particular, external (global) synchronization of VLSI circuits, as it is common practice up to now, at frequencies beyond 100 GHz is relatively impractical, since the small relative time differences necessary for this clocking procedure can no longer be guaranteed over larger distances. In distributing the global clock signal varying delay times may appear that can result in a clock skew. Furthermore, the signal pulses themselves may have different delays. Fortunately, clock pulses for RSFQ cells are physically identical to the signal pulses, and hence can be generated inside RSFQ circuits. Thus, the external global synchronization can be complemented and sometimes replaced by very convenient ***local self-timing***.

A number of asynchronous clocking schemes have been proposed[81] but have not yet been implemented in complex circuits. Data-driven self timing was tested with success for the data exchange between two shift registers at data rates up to 20 GBit/s.[82] Furthermore, in projects aiming at high speed data switches, a clock recovery circuit[83] has been tested successfully at frequencies up to 35 GHz. In the same project, an underdamped long Nb/$AlO_x$/Nb junction was tested as soliton oscillator SFQ clock achieving a linewidth of 38 kHz at 12 GHz[84].

In contrast to the latching voltage state logic the non-latching RSFQ logic does not require an ac power supply. As for semiconductor logic, a much more simple dc power supply is sufficient.

### 5.3.5 Maximum Speed

The probably most impressive figure of merit of RSFQ cells is their extremely high operation speed. Discussing the maximum speed we have to consider the logic delay of RSFQ circuits. For timed circuits such as RSFQ elementary cells, the logic delay is defined as the minimum value of the clock period for which the cell operates correctly. Numerical simulations show that for a typical RSFQ cell, this delay is of the order of $6\pi\tau_{\mathrm{RL}}$ with (compare (5.2.3))

$$\tau_{RL} = \frac{\Phi_0}{2\pi I_c R} . \tag{5.3.2}$$

[81] K. Gaj, Proc. of ISEC 1997, Vol. 2, p. 299 (1997).
[82] Z. J. Deng, Proc. of ISEC 1997, Vol. 2, p. 332 (1997).
[83] V. Kaplunenko, V. Borzenets, N. Dubash, and T. Van Duzer, *Superconducting single flux quantum 20 Gb/s clock recovery circuit*, Appl. Phys. Lett. **71**, 128 (1997).
[84] Y. M. Zhang, V. Borzenets, V. K. Kaplunenko, and N. B. Dubash, *Underdamped long Josephson junction coupled to overdamped single-flux-quantum circuits*, Appl. Phys. Lett. **71**, 1863 (1997).

Here, $R$ is the total normal resistance given by the parallel connection of the shunt resistance $R_L$ and the normal resistance of the junction. We have to take into account that the McCumber parameter

$$\beta_C = \frac{2\pi}{\Phi_0} I_c R^2 C = \frac{2\pi}{\Phi_0} J_c R^2 C_s \tag{5.3.3}$$

can be unity at maximum to have an overdamped junction. With $\beta_C = 1$ we obtain

$$\tau_{\mathrm{RL}} = \frac{\Phi_0}{2\pi I_c} \sqrt{\frac{\Phi_0 I_c C}{2\pi}} \propto \sqrt{\frac{C}{I_c}} \ . \tag{5.3.4}$$

Because $I_c$ is determined by thermal fluctuation stability of the RSFQ circuits requiring $I_c \sim 100\,\mu$A at $T = 4.2$ K, $\tau_{\mathrm{RL}}$ is determined solely by $C$. Since both $C$ and $I_c$ scale with the junction area, one can reduce $C$ by reducing the junction area. In order to keep $I_c$ at the required value of about $100\,\mu$A at the same time one has to increase the current density of the junctions. We see that we need high current density Josephson junctions with small junction area.

For standard niobium trilayer technology the characteristic time $2\pi\tau_{\mathrm{RL}}$ expressed in ps roughly coincides with the linear size of Josephson junctions expressed in $\mu$m. This means that for a $3\,\mu$m technology $2\pi\tau_{\mathrm{RL}} \sim 3$ ps and a typical elementary cell can operate at clock frequencies of the order of 100 GHz. If submicron technology is employed, external shunting of the junctions may become unnecessary, and the operation frequency may approach 500 GHz. At the end, the limiting frequency is the gap frequency $\hbar/\Delta$ corresponding to about 0.5 ps for Nb.

### 5.3.6 Power Dissipation

The power dissipation of RSFQ switches is similar to that of the Josephson switches discussed in section 5.2.2. The energy dissipated per switching process can be estimated to $E_{\mathrm{diss}} \simeq \int I_c V dt$. With $I_c \simeq 100\,\mu$A and $\int V dt = \Phi_0 = 2 \times 10^{-15}$Vs we obtain the very small value of $E_{\mathrm{diss}} \simeq 2 \times 10^{-19}$J.

We note however, that the power consumption of real RSFQ cells is determined not by the energy dissipation inside the Josephson junctions, but by the dissipation in dc supply resistors used for the biasing network. This power dissipation is of the order of $1\,\mu$W per gate. Nevertheless, this value is also slightly lower than that for latching Josephson logic cells.

### 5.3.7 Prospects of RSFQ

There are several potential applications of RSFQ circuits that will be only briefly addressed in the following. Table 5.4 contains a list of possible applications of superconductor digital circuits with the estimated number of required junctions giving the complexity of the circuits.

#### Analog-to-Digital Converters

The simplest and hence the most immediate application of RSFQ technology is analog-to-digital conversion. The reasons for this is obvious: The extremely high switching speed of the Josephson junctions can provide a very short aperture time $\tau_a$ and hence a very high resolution $\varepsilon = 1/2^n = (\pi f_{\mathrm{N}} \tau_a)^{-3/2}$ of the AD converter.[85] Here, $f_{\mathrm{N}}$ is the Nyquist frequency (compare section 5.4.1).

[85] V.K. Semenov, *Digital to analog conversion based on processing of the SFQ pulses*, IEEE Trans. Appl. Supercond. **AS-3**, (1993).

Table 5.4: Possible applications of superconductor digital circuits (source: SCENET 2001).

| **application** | no. of JJs | estimated market size |
|---|---|---|
| integrated SIS receivers with correlator | $10^6$ | small |
| digital multichannel SQUID arrays | $10^5$ | medium |
| dc voltage standards | $10^4$ | small |
| ac voltage standards digital synthesizer | $10^5$ | medium |
| A/D converters | $10^4$ | large |
| D/A converters | $10^3$ | medium |
| dc/ac quantum voltmeters | $10^5$ | large |
| time-digital converters | $10^3$ | medium |
| digital SFQ test circuits for rf-metrology | $10^3$ | medium |
| frequency dividers, digital frequency meters | 500 | medium |
| transient recorders | $10^4$ | medium |
| TeraFLOP workstation | $10^6$ | medium |
| PetaFLOP computer | $10^9$ | ?? |

### Digital SQUIDs

The effective digital filtering described above can be also used for the development of digital SQUIDs which can combine the high sensitivity of analog SQUIDs with a much higher slew rate, linearity and a virtually unlimited dynamic range.[86] Also, the sensitivity is somewhat improved because of the lower noise contribution of the readout electronics. The advantages of the digital SQUID are essential for portable and open environment sensor systems, e.g. for medical diagnostics and imaging, for non-destructive testing (NDE) of materials and for geophysical surveying. Furthermore, digital SQUIDs will certainly relax constraints regarding system design for other applications (e.g. MEG, where shielding is a significant part of the costs). The digital interface with room-temperature electronics will also make digital SQUIDs attractive for gradiometry involving a large baseline or operating at some distance from the ground, in e g geophysical surveying or oil prospecting.

### Digital Signal Processing

A further promising application of RSFQ circuits is digital signal processing, because many algorithms in this field can be implemented with relatively small on-chip memory. A typical example of such processing is digital filtering.[87] In general, RSFQ circuits could extend the well-known complex methods of digital signal processing from acoustic frequencies (tens of kHz) to radio-frequencies (tens and hundreds of MHz) typical for bandwidths of radar, TV, and communication systems.

### Computing

In contrast to digital signal processing, an universal von Neumann-type computer represents a difficult system to be improved by RSFQ technology. The reason is that such a system relies on frequent data

[86] S.V. Rylov, *Analysis of high-performance counter-type A/D converters using RSFQ logic/memory elements*, IEEE Trans. Magn. **MAG-27**, 2431-2434 (1991).

[87] *VLSI and Modern Signal Processing*, S.Y. Kung, H.J. Whitehouse, T. Kailath, eds., Prentice-Hall, Englewood Cliffs, New York (1985).

Table 5.5: Performance of various RSFQ based circuits.

| circuit type | circuit metric(s) |
|---|---|
| toggle flip flop | 144 GHz |
| 4-bit shift register | 66 GHz |
| 6-bit flash ADC | 20 GHz |
| 1:8 demultiplexor (synchronous) | 20 Gb/s |
| 1-bit half-adder | 23 GHz |
| $8 \times N$ bit serial multiplier | 16 GHz |
| 128-bit auto-correlator | 16 GHz |
| 2-bit counter | 120 GHz |
| 1-kbit shift register | 19 GHz |
| 6-bit transient digitizer | 16 Gb/s |
| 1:2 demultiplexor | 95 Gb/s |
| 2-bit full-adder | 13 GHz |
| 14-bit digital comb filter | 20 GHz |
| time-to-digital converter | 31 GHz |

exchange between the processor and the memory. Here, the exchange rate is limited by at least the speed of light (delay time of about 100 ps for a distance of 1 cm) and by today's chip packaging technologies (about 1 ns for data transfer to/from the chip). Direct implementation of such a computer using the RSFQ logic and an existing superconductor memory would probably give a system some 10 times faster than those achievable with semiconductor technologies. It is of course questionable, whether this advantage is sufficient to switch to superconductor technology with its necessity for helium refrigeration. The key problem for superconducting circuits will always be the advancing semiconducting competition. Here, the challenge for superconducting circuits is the fact that a new technology not only has to match the current semiconductor performance but rather has to greatly surpass the performance that may be anticipated for the next 5 to 10 years.

However, there is a general demand from telecommunication and computer area for above 100 GHz systems. For traditional three-terminal semiconducting transistor devices a cutoff frequency approaching 1 THz is needed to achieve a throughput of the order of 100 GHz for small application specific ICs (ASICs). Such performance requirements are beginning to reach the limits of the physical properties of semiconductors[88,89]. Furthermore, it has been noted that the rate of innovation in semiconductor materials and devices has dramatically slowed down with very marginal improvements in device speed.[90] RSFQ technology, based on low-temperature superconductors, has the potential to leapfrog the performance of traditional silicon and III-V compound semiconductors. Simple circuits have been demonstrated with speeds in excess of 750 GHz,[91,92] and complex medium-scale integrated circuits (ICs) operated at 30 GHz[93,94] with performance up to 200 GHz projected in the not-too-distant future.[95] These achieve-

[88] M. Schulz, *The end of the road for silicon?*, Nature **399**, 729 (1999).

[89] P.A. Packan, *Device Physics: Pushing the Limits*, Science **285**, 2079 (1999)

[90] See for example *The International Technology Roadmap for Semiconductors*, Semiconductor Industry Association (1999).

[91] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, *Rapid single flux quantum T-flip-flop operating up to 770 GHz*, IEEE Trans. Appl. Supercond. **AS-9**, 3212-3215 (1999).

[92] W. Chen, A. V. Rylyakov, Vijay Patel, J. E. Lukens, and K. K. Likharev, *Superconductor digital frequency divider operating up to 750 GHz*, Appl. Phys. Lett. **73**, 2817 (1998)

[93] D. K. Brock, *RSFQ technology: Circuits and systems*, Int. J. High Speed Electron. Syst. **11**, 307-362 (2001).

[94] A. F. Kirichenko, S. Sarwana, D. Gupta, I. Rochwarger, and O. A. Mukhanov, *Multi-channel time digitizing system*, IEEE Trans. Applied Supercond. **AS-13**, 454-458 (2003).

[95] A. M. Kadin, C. A. Mancini, M. J. Feldman, and D. K. Brock, *Can RSFQ logic circuits be scaled to deep submicron*

ments represent faster demonstrated electronic circuit speeds than any other technology has predicted to date, even through computer simulations. Prototype RSFQ circuits made with modest research-grade 2-3 $\mu$m linewidth niobium (Nb) fabrication processes have demonstrated circuits such as those shown in Table 5.5.

***PetaFLOP supercomputers*** are a class of massively parallel processing computer architectures, in which RSFQ processors, an RSFQ-based crossbar switch core and Josephson transmission line (JTL) interconnects are essential enabling technology components. One million 1 GHz processors are needed to work in parallel, accessing each other and a large semiconductor memory bank (in the order of 30 terabytes) through a very fast central crossbar switch structure. The task of building a computer capable of $10^{15}$ floating point operations per second (FLOPS) would be virtually impossible without RSFQ technology for, above all, power consumption reasons.

On the long run RSFQ circuits may be the ideal readout and operation circuits for ***superconducting quantum computers***. Cooling to liquid Helium temperatures in such cases can be tolerated, since the quantum performance needs such cooling anyway.

### 5.3.8 Fabrication Technology

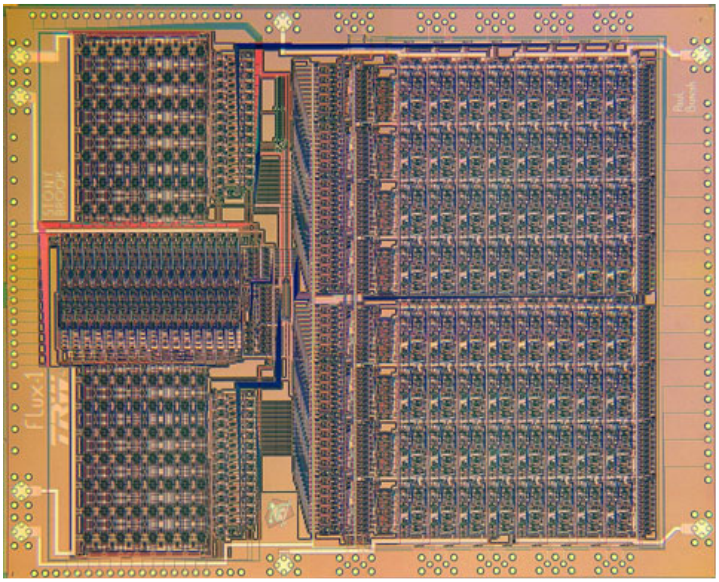

Figure 5.26: First superconducting 20 GHz 8-bit RSFQ microprocessor built in 1.75 $\mu$m Nb-technology designed at SUNY Stony Brook and fabricated using TRW's Nb-trilayer technology ("FLUX-1"). The MPU which uses 16 word instruction memory is fabricated from 70,000 Josephson junctions, consumes 14 mW and is designed to operate at $20-22$ GHz.

As discussed above the delay time of RSFQ gates is proportional to $\sqrt{C/I_c}$. Since for $I_c$ there is a lower bound of about 100 $\mu$A due to thermal fluctuation problems, one is trying to increase the critical current density $J_c$ of the Josephson junctions. This allows to reduce the junction area and hence the capacitance at the same $I_c$ value. However, increasing the critical current density to values above $10^4$ A/cm$^2$ requires very thin tunneling barriers and usually results in an increased $I_c$ spread due to problems with pinholes.

Until today RSFQ circuits with a complexity of $> 1\,000$ Nb/AlO$_x$/Nb junctions have been realized for digital filter and correlator circuits.[96] A-to-D and D-to-A converters with a complexity of about 2 000

*dimensions?*, IEEE Trans. Appl. Supercond. **11**, 1050-1055 (2001).

[96] S.V. Polonsky, Proc. of ISEC 1997, H. Koch and S. Knappe (eds.), Vol. **1** (1997) p. 125.

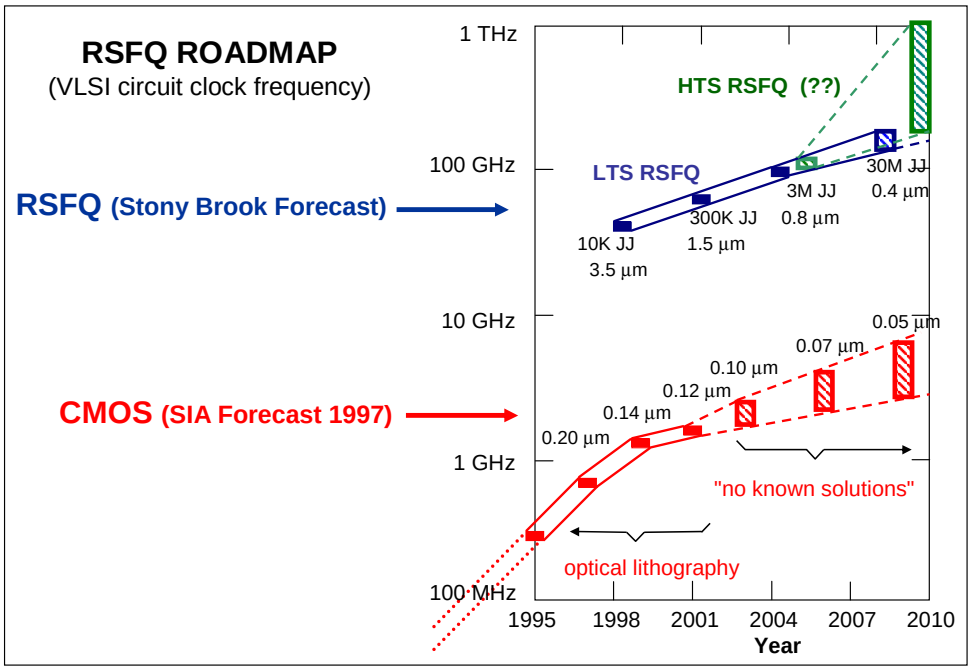


Figure 5.27: Roadmap for RSFQ digital electronics (as projected by K. K. Likharev, SUNY Stony Brook) compared to the SIA forecast for semiconducting CMOS electronics. The numbers below the symbols denote the technology linewidth. The major obstacle for advancing semiconducting electronics above several GHz is the high power dissipation.

junctions have been realized with performance that challenges the best semiconductor converters. One of the most complex RSFQ circuits fabricated so far is an RSFQ microprocessor consisting of about 70 000 Josephson junctions (see Fig. 5.26). Design methods developed for metallic superconductors and cuprate superconductor based RSFQ circuits, for Nb circuits even cell libraries, permit simulations of fairly complex circuits.

Novel developments in the Nb junction technology provide the shunt resistance for the shunting required to overdamp the junction without extra need of chip area thus paving the way for a VLSI integration level.[97,98] To obtain internally shunted Josephson junctions the use of SNS or SINIS type junctions instead of SIS junctions seems to be advantageous. RSFQ shift registers based on SINIS junction technology already have been fabricated and tested.

### 5.3.9 RSFQ Roadmap

The projected potential of RSFQ circuits and their eventual superiority over semiconductor devices is illustrated in the roadmap for RSFQ digital electronics in Fig. 5.27 (as projected by K. K. Likharev, SUNY Stony Brook). Note that the major obstacle for advancing semiconductor electronics above several GHz is the high power dissipation.

[97] H. Kohlstedt, Proc. of ISEC 1997, H. Koch and S. Knappe (eds.), Vol. 1, p. 254.

[98] M. Maezawa, A. Shoji, *Overdamped Josephson junctions with Nb/AlO$_x$/Al/AlO$_x$/Nb structure for integrated circuit application*, Appl. Phys. Lett. **70**, 3603 (1997).

## 5.4 Analog-to-Digital Converters

Analog-to-Digital Converters (ADCs) are known to have widespread applications in consumer as well as professional electronics such as digital tape recorders, digitizing oscilloscopes, voltmeters, transient recorders etc.. Today, mostly semiconductor ADCs are used. The relentless quest for higher performance of analog-to-digital converters (ADCs) is fundamental to progress in communications, radar, high-speed instrumentation, and sensor applications. For many applications, ADCs are the critical elements that define the architecture and the performance capabilities of the entire system. The present relatively slow progress in ADCs based on conventional silicon technology is no longer capable of matching the current rate of advancements in digital circuits. The ever increasing demand for speed and resolution brought superconducting devices into play. For example, for advanced radar systems 16-bit ADCs with a bandwidth of 10 MHz are required. This performance is very difficult to be achieved with semiconductor ADCs, although these devices are improving steadily. On the other hand, superconductor technology exhibits a set of characteristics uniquely suitable for the implementation of analog-to-digital conversion. It simultaneously includes high switching speed (providing a very short aperture time $\tau_a$ and hence a very high speed and resolution for ADCs), low power, natural quantization, quantum accuracy, high sensitivity, and low noise. Superconductor ADCs have already demonstrated superior performance in the laboratory,[99,100] and are now being developed into high-speed and precision instrumentation and communication systems.[101] The first proposals for a Josephson ADC were made by **Klein** and **Zappe** already in the mid 1970s.[102,103]

Superconducting ADCs are based on the principle of flux quantization in a closed superconducting loop and the fast switching of Josephson junctions.[104,105] Together, these naturally occurring quantum phenomena set the current circulating around a closed superconducting loop with Josephson junctions to be fundamentally periodic in the analog magnetic flux applied to it. That is, the threshold spacing of a superconductive loop is determined with the accuracy of fundamental constants. This natural relationship of analog and digital forms makes superconductor technology especially suitable for ADC implementation. In a practical device the input signal to be measured (e.g. a current or voltage) is converted into a magnetic flux $\Phi$ in the same way as we already have discussed for SQUID sensors in chapter 4 and the corresponding circuit has to determine the integer $m$ satisfying the relation

$$(m-1)\Phi_0 \;\leq\; \Phi \leq m\Phi_0 \ . \tag{5.4.1}$$

In this way the input signal is determined within an accuracy of $\Phi_0/2$. An important fact is that the quantization process relies on a fundamental physical constant and therefore has an inherent precision that is not known for semiconductor devices. Of course there exist various ways to determine the number $m$ and related types of ADCs.

[99] S. B. Kaplan, P. D. Bradley, D. K. Brock, D. Gaidarenko, D. Gupta, W.-Q. Li, and S. V. Rylov, *A superconductor flash digitizer with on-chip memory*, IEEE Trans. Appl. Supercond. **AS-9**, 3020-3025 (1999).

[100] O. A. Mukhanov, V. K. Semenov, W. Li, T. V. Filippov, D. Gupta, A. M. Kadin, D. K. Brock, A. F. Kirichenko, Y. A. Polyakov, and I. V. Vernik, *A superconductive high-resolution ADC*, IEEE Trans. Appl. Supercond. **AS-11**, 601-606 (2001).

[101] O.A. Mukhanov, D. Gupta, A.M. Kadin, V.K. Semenov, *Superconductor Analog-to-Digital Converters*, Proceedings IEEE **92**, 1564-1585 (2004).

[102] M. Klein, *Analog-to-digital converter using Josephson junctions*, in *Digest of Tech. Papers*, Int. Solid-State Circuits Conference, Vol. XX (1977), pp. 202-203.

[103] H.H. Zappe, *Ultrasensitive analog-to-digital converter using Josephson junctions*, IBM Tech. Disclosure Bull. **17**, 3053-3054 (1975).

[104] A. M. Kadin, O. A. Mukhanov, *Analog-to-digital converters*, in *Handbook of Superconducting Materials*, D. Cardwell and D. Ginley eds., Institute of Physics, Bristol, UK (2002), pp. 1815-1824.

[105] J. X. Przybysz, *Josephson analog-to-digital converters*, in *The New Superconducting Electronics*, H. Weinstock ed., Kluwer, Dordrecht, The Netherland (1992), pp. 329-361.

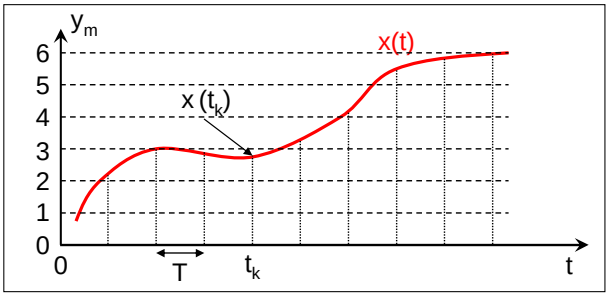


Figure 5.28: Principle of operation of an analog-to-digital converter. The analog signal is sampled at times $t_k = kT$ and the value $x(t_k)$ is mapped onto an integer $y_m = m$.

### 5.4.1 Additional Topic: Foundations of ADCs

#### Principle of Operation

An ADC has to convert an analog signal $x(t)$ into a digital signal. The first operation transforms the time-continuous signal $x(t)$ into a time-discrete signal $x_k = x(t_k)$, where $t_k$ are the points in time at which the signal is sampled. Usually the time intervals between two successive sampling processes are equidistant as shown in Fig. 5.28 and we can write $t_k = kT$. Here, $k$ is an integer and $T$ the sampling period. So far the time-discrete signal is still continuous in amplitude and may be represented by a real number. The second operation now transforms this real number into a set of discrete numbers $y_m$, which most conveniently are represented by a set of integer numbers $y_m = m$. For example, this may be achieved by mapping $x \in [0,0.5]$ onto $y_0 = 0$, $x \in [0.5,1.5]$ onto $y_1 = 1$, $x \in [1.5,2.5]$ onto $y_2 = 2$, and so on. For this particular mapping the spacing between the output bins is just 1. The quantization error $\varepsilon$ is the difference between the input and the output signal, i.e. $\varepsilon \in [-0.5,0.5]$.

For an ADC used for digitizing a voltage signal the output level spacing may be for example $1\,\mu$V. The smallest step in the quantization process is denoted as the ***least significant bit (LSB)***. The quantization error may then be equivalently written as $\varepsilon = \pm 0.5\,\mathrm{LSB}$. A graphical representation of the mapping process is sketched in Fig. 5.29.

#### Resolution

In practice both the range of the input signal $x$ and the number of output values $y_m$ is limited. Furthermore, the number of output values is usually given as a power of 2. If the power is $n$, the ADC is denoted as an $n$-bit converter and the integer numbers 0 to $2^n - 1$ are used (the example shown in Fig. 5.29 represents an 3-bit converter). We can now represent an arbitrary integer number within this range as $x = x_0 2^0 + x_1 2^1 + x_2 2^2 + \ldots + x_{n-1} 2^{n-1}$, where the coefficient $x_0, x_1, x_2, \ldots$ are either 0 or 1. Furthermore, we can scale and offset the input signal in the analog domain so that $x' = ax + b$ (see Fig. 5.29b). If the input signal ranges in the interval $x_{\min} \leq x \leq x_{\max}$ the scaling is used to transform this interval to the range $0 \leq x' \leq 2^n - 1$ and subsequently map this onto the integer numbers 0 to $2^n - 1$. In this way we are taking care about negative signal values.

The resolution of an ADC is given by the number of discrete values it can produce. It is usually expressed in bits. For example, an ADC that encodes an analog input to one of 256 discrete values has a resolution of eight bits, since $2^8 = 256$. If we are digitizing for example a voltage signal, the resolution can also be defined electrically, and expressed in volts. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete values. For example, if the full scale

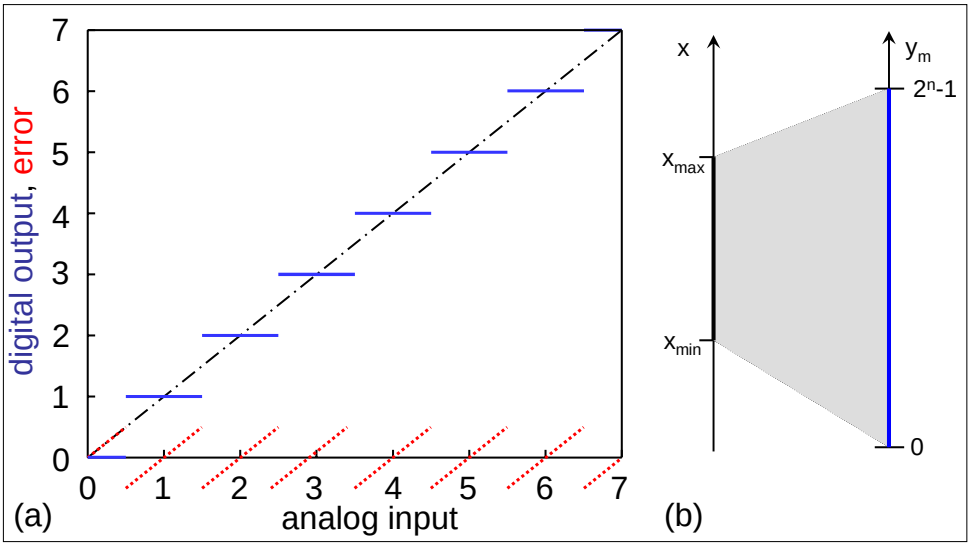


Figure 5.29: (a) Sketch of the analog-to-digital conversion process assuming 8 available output levels. The full lines represent the output signal, the dash-dotted line the input signal, and the dotted line the quantization error. (b) Mapping of the input signal range onto the available range of digits.

measurement range is 0 to 10 V and the ADC resolution is 12 bits ($2^{12} = 4096$ quantization levels), then the ADC voltage resolution is: $(10-0)/4096 = 0.00244\,\text{V} = 2.44\,\text{mV}$. If the full scale measurement range is -10 to +10 V and the ADC resolution is 14 bits ($2^{14} = 16384$ quantization levels), then the ADC voltage resolution is: $[10-(-10)]/16384 = 20/16384 = 0.00122\,\text{V} = 1.22\,\text{mV}$.

The resolution of the ADC may be limited by the signal-to-noise ratio of the signal in question. If there is too much noise present in the analog input, it will be impossible to accurately resolve beyond a certain number of bits of resolution, the so-called ***effective number of bits (ENOB)***. While the ADC will produce a result, the result is not accurate, since its lower bits are simply measuring noise. The S/N ratio should be $20\log_{10}2 = 6.02\,\text{dB}$ per bit of resolution required.

### Accuracy

Accuracy depends on the error in the conversion. This error is measured in a unit called the LSB. For example, for a 8 bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%. The quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. The magnitude of the quantization error at the sampling instant is between zero and half of one LSB.

The instances $t_i$ of the sampling process are determined by the sampling period $T$. In the general case, the original signal is much larger than one LSB. When this happens, the quantization error is not correlated with the signal, and has a uniform distribution. Then, the quantization error can be treated as white noise.

Its root mean square (rms) value is the standard deviation of this distribution, given by[106]

$$\varepsilon_{\rm rms} \;=\; \frac{1}{\sqrt{12}}{\rm LSB} \;\simeq\; 0.289\,{\rm LSB}\;. \tag{5.4.2}$$

**Signal-to-Noise Ratio:** For an $n$-bit converter the peak-to-peak amplitude is $A_{\rm pp} = 2^n - 1$. If we assume a sinusoidal input signal, then the rms value of its amplitude is given by $A_{\rm rms} = A_{\rm pp}/2\sqrt{2}$. The signal to noise ratio (SNR) for an ADC is defined as the so-called dynamic range of the ADC and is equal to $A_{\rm rms}/\varepsilon_{\rm rms}$. Usually, the SNR is expressed in decibels. For $n > 5$, we can use $2^n - 1 \simeq 2^n$ and obtain

$$\mathrm{SNR_{ADC}(dB)} \;=\; 20\log_{10}\left(\frac{A_{\rm rms}}{\varepsilon_{\rm rms}}\right) \;\simeq\; 20\log_{10}\left(2^n\sqrt{3/2}\right) \;=\; 6.02\,n + 1.76\;. \tag{5.4.3}$$

Putting in some numbers we obtain a dynamic range of 98.1 dB for a 16-bit ADC, which is often used in consumer electronics such as compact-disc players. Of course, besides the quantization error there may be additional errors arising from the analog part of the converter (inaccuracy of the scaling constants $a$ and $b$).

### Sampling Rate

The analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the ***sampling rate*** or ***sampling frequency*** of the ADC. A continuously varying bandlimited signal $x(t)$ can be sampled. That is, the signal values at intervals of time $T$ (the sampling time) are measured and stored. Then, the original signal can be exactly reproduced from the discrete-time values by an interpolation formula. The accuracy is, however, limited by quantization errors. The successful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the ***Shannon-Nyquist sampling theorem***[107] also known as

[106] The quantization noise $\varepsilon(n)$ is treated as a random variable in the interval $[-q/2,+q/2]$. It therefore has the probability density function $p_\varepsilon(x) = 1/q$ for $|x| \le q/2$ and $p_\varepsilon(x) = 0$ for $|x| > q/2$. Thus, the probability that a given roundoff error $\varepsilon(n)$ lies in the interval $[x_1,x_2]$ is given by

$$\int_{x_1}^{x_2} p_\varepsilon(x)dx \;=\; \frac{x_2 - x_1}{q}$$

with $x_1$ and $x_2 \in [-q/2,+q/2]$. We can now calculate the variance of the random variable $\varepsilon(n)$ which we assume to be uniformly distributed on $[-q/2,+q/2]$. We obtain

$$\sigma_\varepsilon^2 \;=\; \int_{-q/2}^{q/2} x^2\,\frac{1}{q}\,dx \;=\; \frac{1}{q}\frac{x^3}{3}\Big|_{-q/2}^{q/2} \;=\; \frac{q^2}{12}\;.$$

Since in our case $q = 1$ we obtain the variance $1/12$. For sampled processes the sample variance is proportional to the average power in the signal. Finally, the square root of the sample variance (the rms level) is sometimes called the standard deviation of the signal. However, this notation is only correct if the random variable has a Gaussian probability density function.

[107] The WKS theorem was formulated by Claude Elwood Shannon in 1948 as the starting point for his theory on the maximum bit rate in a frequency limited transmission channel. He was using results of Harry Nyquist (1928) on the transmission of number series by trigonometric polynoms and the theory of the cardinal functions by Edmund Taylor Whittaker (1915) and his son John Macnaughten Whittaker (1929). Independently, the sampling theorem was introduced by the Russian scientist Wladimir Alexandrowitsch Kotelnikow in 1933. However, this was noticed in the western literature only in the 1950s. The sampling theorem says that a continuous signal with minimum frequency 0 and maximum frequency $f_{\rm max}$ has to be sampled by a frequency larger than $f_{\rm sam} > 2f_{\rm max}$ in order to be reconstructed from the time-discrete signal without loss of information. The Nyquist-Shannon sampling theorem is relevant for digitizing. The characteristic frequency $f_N = \frac{1}{2}f_{\rm sam}$ is denoted as the Nyquist frequency.

Nyquist-Shannon-Kotelnikov, Whittaker-Shannon-Kotelnikov, Whittaker-Nyquist-Kotelnikov-Shannon, WKS, etc.[108,109,110,111]

As the input signal $x(t)$ varies in time, a sample of it is taken at a certain moment $t_s$. However, in practice the sampling process takes a finite amount of time given by the so-called aperture time $t_a$ or acquisition time for sample & hold. This aperture time has to incorporate the aperture times of the different comparators as well as of the spread in sampling times. In practice, an input circuit called a sample and hold performs this task (in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input). Many ADC integrated circuits include the sample and hold subsystem internally.

Obviously, if the input signal changes by more than one LSB during the aperture time, the error in the conversion process would exceed the resolution of the ADC. In order to avoid this we directly obtain an upper limit for the bandwidth of the ADC, which is directly related to the aperture time. For a harmonic signal $S = \sin 2\pi ft$ with frequency $f$ and amplitude 1 the maximum slew rate is $2\pi f \cos 2\pi ft = 2\pi f$. The analog signal needs the minimum time $1/(2^n - 1)\pi f$ to slew by an amount equal to the LSB.[112] This time must be larger than the aperture time. Hence, the frequency of the input signal must satisfy the condition

$$f \leq f_B = \frac{1}{(2^n - 1)\,\pi t_a} \tag{5.4.4}$$

to ensure that the error does not exceed $\pm 0.5$ LSB. Here, $f_B$ is the input bandwidth of the ADC. Expression (5.4.4) immediately shows that the product $2^n f_B \simeq 1/t_a$, that is, the aperture time is limiting the performance of the ADC. If we want to increase the bit resolution, we have to reduce the bandwidth and vice versa. We also see that the performance of an ADC is the better the shorter the aperture time.

We note that even in the case of zero aperture time, errors may arise if the input bandwidth is too high. If the signal with frequency $f$ is sampled at a frequency $f_{\text{sam}}$, mixing products at $f_{\text{sam}} \pm f$, $2f_{\text{sam}} \pm f$, etc. appear in the output spectrum. Therefore, the input bandwidth $f_B$ is not allowed to exceed $f_{\text{sam}}/2$. If a signal is sampled at twice the input bandwidth we say that it is sampled at the ***Nyquist rate*** $f_{\text{sam}} = 2f_N = 2f_B$.[113]

We can summarize our discussion by stating that there are two distinct aspects of the analog-to-digital conversion process: ***sampling*** and ***quantization***, which deal with discretization in time and in magnitude,

[108] Claude Elwood Shannon, *Communication in the Presence of Noise*, Proc. IRE, Vol. **37**, No. 1 (1949), see also Proc. IEEE, Vol. **86**, No. 2, (1998).

[109] J. M. Whittaker, *The Fourier theory of the cardinal functions*, Proc. Edinburgh Math. Soc. **1** (1929).

[110] V. A. Kotelnikow *On the transmission capacity of ether and wire in electrocommunications*, Izd. Red. Upr. Svyazzi RKKA (1933).

[111] Harry Nyquist, *Certain Topics in Telegraph Transmission Theory*, Trans. Amer. Inst. Elect. Eng. **47**, 617-644 (1928); see also Proc. IEEE, Vol. **90**, No. 2 (2002).

[112] Here we have taken into account that the peak-to-peak amplitude of a harmonic signal with amplitude 1 is just 2.

[113] The Nyquist frequency $f_N$ is half the sampling frequency for a signal. It is sometimes called the critical frequency. The sampling theorem tells us that aliasing can be avoided if the Nyquist frequency is at least as large as the bandwidth of the signal being sampled (or the maximum frequency, if the signal is a baseband signal).
In principle, a Nyquist frequency equal to the signal bandwidth is sufficient to allow perfect reconstruction of the signal from the samples. However, this reconstruction requires an unrealizable filter that passes some frequencies unchanged while suppressing all others completely. When realizable filters are used, oversampling is necessary to accommodate the practical constraints on anti-aliasing filters. Even with oversampling, the Nyquist frequency is half the sampling frequency.
For example, audio CDs have a sampling frequency of 44,100 Hz. The Nyquist frequency is therefore 22 050 Hz, which represents the highest frequency the data can produce (again if the anti-aliasing filter is perfect). For example, if the chosen anti-aliasing filter (a low-pass filter in this case) has a transition band of 2 000 Hz then the cut-off frequency should be at 20 050 Hz to yield a signal with no power at frequencies of 22 050 Hz and greater. Again, because realizable filters are not perfect, the frequencies greater than 22 050 will still have power except the aliasing they will produce is minimal.

respectively. The quantization process introduces some error or "quantization noise" into the system. Of course, this is in addition to any noise present in the signal, as well as other noise sources, such as jitter in the sampling clock. Even if the quantization is precise, the clock frequency will limit the bandwidth of a signal in the digital domain. According to the Nyquist sampling theorem, a signal that is sampled at a frequency can accurately represent an analog signal with bandwidth up to the Nyquist frequency $f_N = f_{\rm sam}/2$.

### Aliasing

All ADCs work by sampling their input at discrete intervals of time. Their output is therefore an incomplete picture of the input signal. By looking at the output, there is no way of knowing what the input was doing between one sampling instant and the next. If the input is known to be changing slowly compared to the sampling rate, then it can be assumed that the value of the signal between two sample instants was somewhere between the two sampled values. If, however, the input signal is changing fast compared to the sample rate, then this assumption is no longer valid.

If the digital values produced by the ADC are, at some later stage in the system, converted back to analog values, it is desirable that the output of the digital to analog converter (DAC) is a faithful representation of the original signal. If the input signal is changing much faster than the sample rate, then this will not be the case, and spurious signals called ***aliases*** will be produced at the output of the DAC. The frequency of the aliased signal is the difference between the signal frequency and the sampling rate. For example, a 10 kHz sinewave being sampled at 9 kHz would be reconstructed as a 1 kHz sinewave. This problem is called aliasing. To avoid aliasing, the input to an ADC must be low-pass filtered to remove frequencies above half the sampling rate. This filter is called an ***anti-aliasing filter***.

### Oversampling

The fabrication of ADCs with a large number of bits requires high precision components in order to define the transition points between the bits in an adequate way. Therefore, a variety of clever tricks to reduce the number of high precision components and thereby the costs have been developed.[114] We only briefly address the oversampling technique.

The term oversampling is used, if the sampling rate is larger than the Nyquist rate $f_N$. The oversampling rate is defined as

$$\text{OSR} \;=\; \frac{f_{\rm sam}}{f_N}\;. \tag{5.4.5}$$

For example, if an audio signal of 20 kHz bandwidth is sampled at a rate of 160 kHz we have with $f_N = 2f_B$ an OSR of four. The obvious advantage is that one can significantly reduce the requirement for the anti-alias filter leading to a significant cost reduction.

A further advantage is the reduction of quantization noise within the input bandwidth. Usually, signals are sampled at the minimum rate required, for economy, with the result that the quantization noise introduced is white noise spread over the whole pass band of the converter. If a signal is sampled at a rate much higher than the Nyquist frequency and then digitally filtered to limit it to the signal bandwidth, the signal-to-noise ratio due to quantization noise will be lower than in the case where the whole available band had been used. With this technique, it is possible to obtain an effective resolution larger than that provided by the converter alone by randomizing the quantization noise over a larger bandwidth. The

[114] D.F. Hoeschele, *Analog-to-digital and digital-to-analog conversion techniques*, Wiley, New York (1994).

power $\varepsilon_{\text{rms}}^2$ of the quantization noise is now spread over the bandwidth $f_{\text{sam}}/2$ instead of only $f_B$. This leads to a reduction of a factor $\sqrt{\text{OSR}}$ in the quantization noise of the ADC and the SNR is increased by $10\log(\text{OSR})$ dB. At 4-times oversampling this leads to an improvement of 6.02 dB or equivalently we gain an extra bit of dynamic range. An interesting aspect is to use a one-bit converter to arrive at a dynamic range of 16 bit. The advantage of a one-bit ADC would be that it is highly linear and hardly requires any costly components. The only penalty we have to pay is the increase of the sampling rate, the complexity of the digital part and processing speed. For example, digital filtering is required to remove the noise not lying in the input bandwidth. Of course, the physics behind oversampling is just signal averaging. If for example the sampling frequency is 16 times the Nyquist frequency, one can measure 16 times as often in the same time window. This improves the SNR by $16/\sqrt{16} = 4$ and one gains two bits in dynamic range.

### 5.4.2 The Comparator

A key element of any ADC is the comparator, which compares the analog input signal to some reference signal. If the input signal is smaller than the reference signal it generates a "0", if it is larger than the reference signal, it generates a "1". The reference signal value is set just at one of the transition points $x = 0.5, 1.5, 2.5, \ldots$ (see Fig. 5.29). It is evident that there is some uncertainty in the comparison process just around the transition point due to noise. That is, in a small interval around the reference signal level the output is undetermined. This sets a lower bound for the resolution of the ADC, since two neighboring quantization levels can no longer be distinguished if they are too close.

#### Semiconductor Comparator

A semiconductor comparator is nothing else than a high gain amplifier with a clipped output (cf. Fig. 5.30a). If the input signal is larger or smaller than the reference signal, the small difference is amplified by such a high factor that the resulting output signal effectively is given by the clipped low or high level signal.

#### Superconductor Comparator

In a superconductor comparator flux quantization in a superconducting loop is used. In the one-junction comparator shown in Fig. 5.30b the input signal is compared to the maximum supercurrent $I_s^m$ of a circuit consisting of a superconducting loop with inductance $L$ and a quantizer Josephson junction $\text{J}_Q$ with critical current $I_c$. If the input signal is smaller than the maximum supercurrent $I_s^m$, the circuit stays in the superconducting state and the output signal is zero. In this case most of the current is flowing across the junction and not the inductor, since this would generate too much flux and result in a lower $I_s^m$. This state can be represented by an equal current through the junction and the inductor plus a clockwise circulating current $I_{\text{circ}}$. If in contrast the input signal is increased above $I_s^m$, the junction will switch into the voltage state. A flux quantum enters the loop and a SFQ voltage pulse is generated at the output due to the $2\pi$ phase slip of the quantizer junction. As a result of the counter-clockwise circulating current associated with the trapped flux quantum the effective current across the junction is reduced below $I_s^m$ again and the circuit again resides in the superconducting state. That is, the circuit generates a single SFQ voltage pulse of height $I_c R_N$ and duration $\Phi_0/I_c R_N$ at the output, if the signal current exceeds the reference value. Increasing the current further, the next flux quantum will enter at the next threshold value resulting in a further SFQ pulse. If the output pulses are fed into a counter, a so-called counting ADC is achieved. Here, an additional output pulse corresponds to a change by a discrete amount in the analog signal.

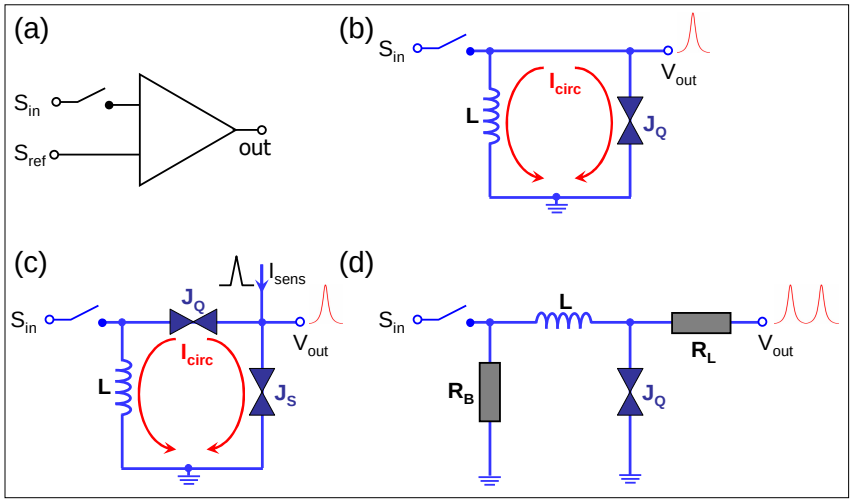


Figure 5.30: (a) Semiconductor comparator. (b) Superconducting one-junction SQUID comparator. Depending on the flux state of the loop the circulating current is clockwise or counterclockwise. (c) Superconducting quasi-one-junction SQUID comparator (QOS). (d) Voltage to frequency quantizer.

Instead of the output SFQ pulses, the direction of the circulating loop current $I_{\rm circ}$ may be sensed. In order to do so an extra sense junction $J_S$ is introduced as shown in Fig. 5.30c. In this way a quasi-one-junction SQUID (QOS) may be obtained.[115] The critical current of the sense junction must be larger than that of the quantizer junction, since it should not switch if the input signal is applied. The direction of the loop current is sensed by applying a sensing current pulse $I_{\rm sens}$ to the circuit. If $I_{\rm sens}+I_{\rm circ} > I_{c,S}$, a SFQ voltage pulse is generated at the output. For $I_{\rm sens}+I_{\rm circ} < I_{c,S}$ nothing happens. That is, the presence or absence of an output voltage pulse indicates whether the circulating current is clockwise or anti-clockwise. Note that the use of a sense junction is a prerequisite if the circuit is used in a parallel converter scheme. Here, the status of several comparators has to be sensed at exactly the same time. The simple one-junction comparator does not satisfy this condition, since the output pulse is generated as soon as the input signal exceeds the reference signal. In the QOS the result is stored in the loop and then asked for by the sensing current pulse at some specific time.

A further type of counting ADC can be realized by the quantizer circuit shown in Fig. 5.30d. The circuit is used to generate discrete voltage pulses in response to an input signal. In contrast to the circuit of Fig. 5.30b, now a train of pulses is generated at a rate proportional to the signal amplitude. We already have seen that a voltage biased Josephson junction acts as a voltage controlled oscillator with $V/f = 483.6\,\mathrm{MHz}/\mu\mathrm{V}$. Because the Josephson junction has a low impedance, it needs a bias resistor $R_B$ of the order of mΩ in order for the analog signal to voltage bias the junction. The inductance $L$ is required to block the produced pulses from draining into $R_B$. Instead the pulses pass to the counter through the resistance $R_L$ which damps the junction ($\beta_C < 1$). The ADC is capable to measure a dc voltage. The resolution increases with increasing counting time. However, the accuracy cannot be increased arbitrarily due to the finite linewidth of the Josephson frequency. With the thermal voltage noise $S_V = \delta V^2/\Delta f = 4k_BTR_B$ of the small bias resistor and the 2. Josephson equation ($f = 2eV/h$ or $\Delta f = 2e\delta V/h$) the limit of the linewidth is obtained to

$$\Delta f \;=\; \left(\frac{2e}{h}\right)^2 4k_BTR_B \;. \tag{5.4.6}$$

For $R_B = 1\,\mathrm{m}\Omega$ we obtain $\Delta f \sim 100\,\mathrm{kHz}$ at 4 K. The maximum bit accuracy is then $\log_2(F/\Delta f)$, where $F$ is the maximum counting rate. For $F = 50\,\mathrm{GHz}$ we would obtain a bit accuracy of about 16 bit. We note

[115] H. Ko, T. Van Duzer, *A new high speed periodic threshold comparator for use in a Josephson ADC*, IEEE J. Solid-State Circuits **23**, 1017-1021 (1988).

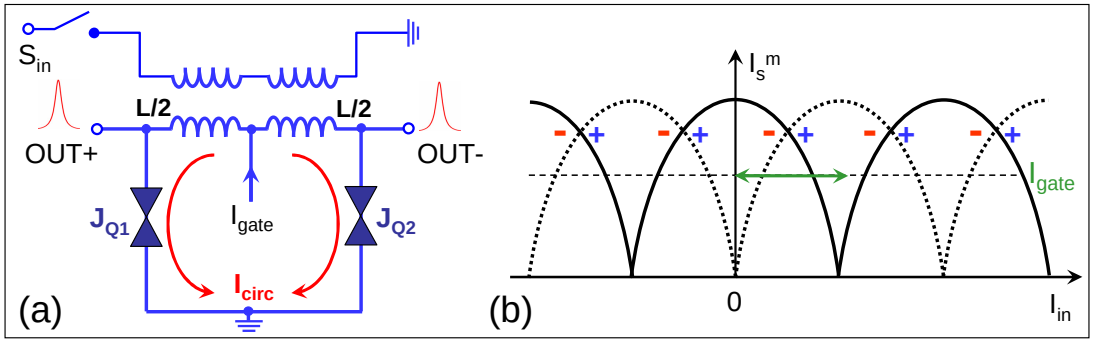


Figure 5.31: (a) Circuit diagram of an incremental quantizer. (b) Threshold characteristic of the incremental quantizer. Whenever the input signal $I_{\rm in}$ increases sufficiently to cross the right-hand side of a mode boundary, the phase of $J_{Q2}$ changes by $2\pi$ and a SFQ pulse is sent out at OUT-. In the same way, whenever $I_{\rm in}$ decreases sufficiently to cross the left-hand side of a mode boundary, the phase of $J_{Q1}$ changes by $2\pi$ and a SFQ pulse is sent out at OUT+.

that the $V/f$ type counting ADC has an extreme nonlinearity close to $V = 0$ due to the strong nonlinearity of the IVC of an overdamped Josephson junction.

One also can implement an incremental comparator by the circuit shown in Fig. 5.31. If the analog signal increases or decreases, the threshold characteristic is crossed in the one or the other direction to a different flux state. This is equivalent to flux quanta entering or leaving the superconducting loop via the quantizer Josephson junctions $J_{Q+}$ and $J_{Q-}$ resulting in SFQ voltage pulses at the outputs OUT+ and OUT-, respectively. One can now use different counters for the two outputs and can determine the incremental change of the input signal in the one or the other direction from the counting rates. The incremental ADC theoretically has a very high linearity, although in practice the linearity will be limited by stray magnetic flux suppressing the critical current of the junctions.

### 5.4.3 The Aperture Time

We already have mentioned that a particular advantage of Josephson junction based ADCs is the very fast switching speed of Josephson junctions. The width of the SFQ pulse is $\Phi_0/I_cR_N \sim 2\,\text{ps}$ for an $I_cR_N$ product of 1 mV, which is in principle achievable e.g. for junctions based on Nb technology. From this we could conclude that for Josephson junction based ADC a bandwidth well above 100 GHz should be possible.

In general the speed and accuracy of any ADC is given by its aperture time

$$t_a = \frac{1}{(2^n - 1)\,\pi f_B} \,. \tag{5.4.7}$$

With the optimum estimate that $t_a$ is set by the switching time of a Josephson junction ($\sim 2\,\text{ps}$) it would be possible to obtain a bandwidth of more than 1 MHz for a 16 bit ADC. Unfortunately, there are other limitations reducing the performance of Josephson junction based ADCs below this fantastic value. However, superconducting ADCs have at least exceeded the performance of the best semiconductor ADCs with further improvement anticipated.[116,117] For example, in an effort to realize a true software-defined radio recently ultra-high-performance superconducting ADCs have been developed that directly convert

[116] T. Van Duzer, *Superconductor Electronics*, IEEE Trans. Appl. Supercond. **7**, 98 (1997).
[117] T. Van Duzer, *Digital Signal Processing*, in *Superconducting Devices*, S.T. Ruggiero, D.A. Rudman eds., Academic Press Inc., San Diego (1990).

RF signals from the antenna to digital baseband with an exceptionally high signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR). The expected performance is 14 to 16 effective bits with an SFDR of over 100 dB and an SNR of 90 dB at 14 bits.

At present the fast switching speed of Josephson junctions cannot be fully used due to several technical hurdles. Firstly, since the junctions are embedded into complex circuits, the actual switching speed of the junction may be larger due to parasitic capacitances and inductances. Secondly, the SFQ pulses do not arrive exactly at the intended moment. This is obvious, if several comparators have to work in parallel and not all sampling pulses arrive simultaneously or not all output pulses will be available at the same time. Another effect that limits the bandwidth is the dynamic hysteresis of the comparator. These hysteresis effects result from the charging and discharging of capacitors and inductors. Note that we have not shown the junction capacitance and parasitic capacitances in Figs. 5.30 and 5.31.

### 5.4.4 Different Types of ADCs

All superconductor ADCs generally fall into two categories: Nyquist-sampling ADCs and oversampling ADCs. An ideal Nyquist ADC samples a bandwidth-limited signal at a sampling rate $f_{\rm sam} = 2f_N$ and provides an accurate digital representation of that signal, with the only error associated with the quantization noise. Most commonly, this Nyquist ADC is composed of a large number of separate quantizers (single-bit comparators), each defining a single quantization level. In practice, the performance of such an ADC is limited by the precision of the quantization levels, which are often determined by resistor values in resistor networks.

In the alternative oversampling ADC approach, the signal is sampled at a frequency $f_{\rm sam} \gg 2f_N$ using a single quantizer. Then feedback techniques and digital filtering are used to decrease the quantization noise and enhance the effective dynamic range. Oversampling ADCs are built using a "delta" or more often a "deltaŰsigma" modulator (sometimes called "sigmaŰdelta").[118] Here, $\Delta$ refers to difference and $\Sigma$ to sum, the discrete analogues of differentiation and integration.

#### Superconducting Nyquist ADCs: Flash Converters

A well-known representative of Nyquist ADCs is the flash converter (see Fig. 5.32). A flash ADC has a comparator that fires for each decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, but usually has only small number of bits. For example, 8 bits of resolution requires 256 comparators and hence a large, expensive circuit.

We note, however, that a superconductor flash ADC based on SQUID comparators provides a unique solution for a strong reduction of circuit complexity and, at the same time, allows faster sampling. Utilizing the periodicity of a SQUID's transfer characteristics in units of $\Phi_0$, an $n$-bit superconductor flash ADC uses only $n$ clocked SQUID comparators.[119]

Fig. 5.32 shows the schematic of a flash ADC. The input signal is successively divided by factors of two and applied to a set of identical comparators, each with periodic thresholds. The output of the first comparator is the most significant bit (MSB) and that of the last comparator is the least significant bit (LSB). In an $n$-bit ADC, the first comparator gets $2^n - 1$ times the current applied to the last comparator. As the input signal increases, each comparator goes through multiple thresholds.

[118] S. R. Norsworthy, R. Schreier, and G. C. Temes, *DeltaŰSigma Data Converters: Theory, Design, and Simulation*, IEEE, New York (1997).

[119] P. Bradley and H. Dang, *Design and testing of quasi-one junction SQUID-based comparators at low and high speed for superconductor flash A/D converters*, IEEE Trans. Appl. Supercond. **AS-1**, 134-139 (1991).

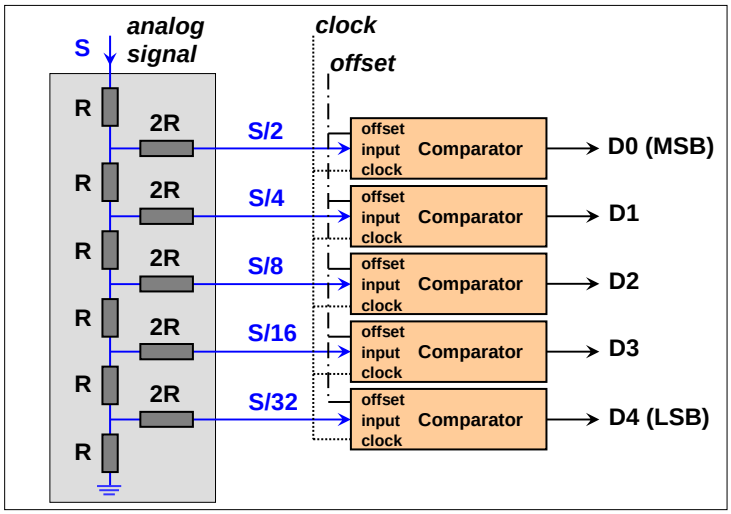


Figure 5.32: Schematic diagram of a 5 bit flash ADC with $n = 5$ SQUID comparators. The $R/2R$ resistor ladder serves for dividing the signal.

Like all multi-comparator ADCs, the superconductor flash ADC is susceptible to mismatched circuit components and other problems such as the resistor ladder, delays in clock and signal paths, and in differences in local magnetic environment. Component mismatches depend on the quality of the IC fabrication process. For correct operation, the analog signal and the sampling clock must be applied simultaneously at each comparator, requiring precise transmission line designs on the signal and clock paths as they travel from the LSB comparator to the MSB comparator. Otherwise, the aperture time would strongly increase resulting in a reduction in the input bandwidth. This can limit the number of bits for a high-speed flash ADC. Based on Nb/$AlO_x$/Nb junctions 6 bit flash-type ADCs have been fabricated and an effective 4 bit resolution has been demonstrated at 5 GHz.[120] Furthermore, 3 effective bits at 20 GHz have been experimentally demonstrated for junctions with $J_c = 2.5\,\mathrm{kA/cm^2}$.[121]

### Counting Converters

Historically, the first Josephson ADCs[122,123] were based on the voltage-to-frequency ($V/f$) conversion utilizing the ac Josephson effect. In this type of ADC, the processes of quantization and sampling are separated. A single Josephson junction acts as a voltage-controlled oscillator (VCO) and produces an SFQ pulse train at a rate proportional to the applied analog voltage as $f = V/\Phi_0$. This is a process of signal magnitude quantization. As shown in Fig. 5.30d, a very small shunt resistor $R_B$ converts input current to a voltage bias across the junction. It is worth noting that there is an inductance (often omitted in diagrams) between the junction and the resistor which prevents the generated SFQ pulses from being shunted. This inductor also forms a SQUID loop (a resistive single-junction interferometer) allowing the realization of implicit feedback and integration functions. The signal sampling process is performed by counting the number of generated SFQ pulses over a time interval (cf. Fig. 5.33), which is controlled by a sampling gate. Overall, this analog-to-digital conversion is equivalent to a low-pass first-order

[120] P. Bradley, *A 6 bit Josephson flash A/D converter with GHz input bandwidth*, IEEE Trans. Appl. Supercond. **AS-3**, 2550-2557 (1993).

[121] S. B. Kaplan, P. D. Bradley, D. K. Brock, D. Gaidarenko, D. Gupta, W.-Q. Li, and S. V. Rylov, *A superconductor flash digitizer with on-chip memory*, IEEE Trans. Appl. Supercond. **AS-9**, 3020-3025 (1999).

[122] J. P. Hurrell, D. C. Pridmore-Brown, and A. H. Silver, *A/D conversion with unlatched SQUID's*, IEEE Trans. Electron Devices **27**, 1887-1896 (1980).

[123] C. A. Hamilton and F. L. Lloyd, *100 GHz binary counter based on dc SQUIDs*, IEEE Electron Device Lett. **3**, 335-338 (1982).

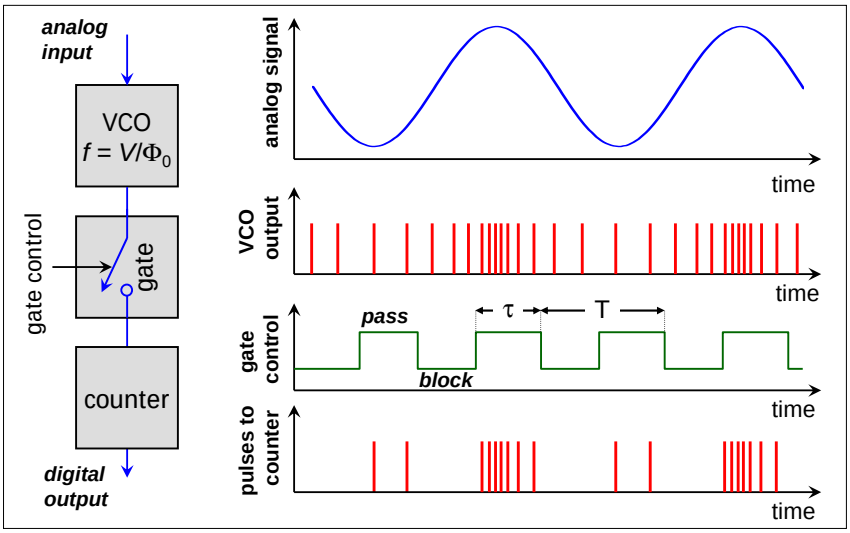


Figure 5.33: Block diagram, input signal, SFQ pulse output of voltage-to-frequency converter (VCO), gate control signals with counting and sampling time intervals ($\tau$ and $T$) controlled by a fast RSFQ logic gate, and resulting SFQ pulses sent to ripple counter (according to M. W. Johnson *et al.*, IEEE Trans. Appl. Supercond. **AS-11**, 607-611 (2001)).

sigmaŰdelta modulation. The pulse counting process is done using toggle flip-flops forming a ripple counter, which are the fastest elements in RSFQ technology. As a result, the digitized voltage averaged over the sampling period is read out from the counter.[124] In order to avoid strong nonlinearities of such a VCO at low input signal, it is necessary to operate the VCO at some input offset. This offset also helps to accommodate positive and negative signals.

In order to increase the sensitivity of the $V/f$ counting-type ADC, one can replace the quantizer junction in Fig. 5.30d by a dc SQUID with a sensitive input transformer biased into the voltage state as a pulse generator.[125,126] This transformer magnetically couples the input signal current (or flux) to a SQUID, which is biased above its critical current. The resultant flux in the SQUID loop produces modulation of the SQUID voltage. Once again, the SQUID produces an SFQ pulse stream, at a frequency that is exactly proportional to the voltage.

In another counting ADC design (flux quantizing or tracking ADC design) the input signal current is coupled into a SQUID loop, which generates one SFQ pulse for each change in flux. Similarly to the $V/f$ ADC, these SFQ pulses can be counted using superconductor digital circuits to reconstruct the signal. This scheme can also be extended to obtain an incremental counting ADC as shown in Fig. 5.31.

### Delta and Sigma-Delta Converters

A so-called delta-encoded ADC has an up-down counter that feeds a digital to analog converter (DAC). The input signal and the DAC both go to a comparator. The comparator controls the counter. The circuit uses negative feedback from the comparator to adjust the counter until the DAC's output is close enough to the input signal. The number is read from the counter. Delta converters have very wide ranges, and high resolution, but the conversion time is dependent on the input signal level.

[124] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, *An architecture of delta sigma A-to-D converters using a voltage controlled oscillator as a multi-bit quantizer*, in Proc. IEEE Int. Symp. Circuits and Systems **1** 389-392 (1998).

[125] O. A. Mukhanov, S. Sarwana, D. Gupta, A. F. Kirichenko, and S. V. Rylov, *Rapid single flux quantum technology for SQUID applications*, Physica C **368**, 196-202 (2002).

[126] S. Sarwana, D. Gupta, A. Kirichenko, T. Oku, C. Otani, H. Sato, and H. Shimizu, *High-sensitivity high-resolution dual-function signal and time digitizer*, Appl. Phys. Lett. **80**, 2023-2025 (2002).

A Sigma-Delta ADC oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a flash ADC after the filter. The resulting signal, along with the error generated by the discrete levels of the flash ADC is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the flash ADC so that it does not appear in the desired signal frequencies. A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. Both superconducting delta and sigma-delta ADCs have been successfully implemented.[127]

[127] O.A. Mukhanov, D. Gupta, A.M. Kadin, V.K. Semenov, *Superconductor Analog-to-Digital Converters*, Proceedings IEEE **92**, 1564-1585 (2004).